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NCR | CDC

ADVANCED SYSTEMS LABORATORY

IPL ARCHITECTURAL OBJECTIVES

ARCHITECTURAL DESIGN AND CONTROL

Doc. No. ASL00404

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APPROVAL

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REVISION DEFINITION SHEET

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1.0 INTRODUCTION

1.1 DEFINITION

These Architectural Objectives are the Advanced Systems Laboratory's formal response to Requirements and Goals established by NCR and COC for an Integrated Product Line.

For purposes of technical program definition, this document will replace the NCR/COC Requirements and Goals, which remains an historic record for amplification.

1.2 MAJOR OBJECTIVES

The major design objectives influencing the Integrated Product Line (IPL) are listed below in relative priority order:

- SPAN OF PRODUCT OFFERING
- RELIABILITY/AVAILABILITY/SERVICEABILITY
- USABILITY
- MIGRATION
- PROTECTION/SECURITY
- STORAGE STRUCTURE

A balance among these general objectives must be maintained. No high priority factor is to be allowed to compromise a lower factor below acceptable levels defined elsewhere in this and successor documents.

1.2.1 SPAN OF PRODUCT OFFERING

The hardware/software system will span a large range ($50,000 MLB and up) of configurations, processing power, and application uses.

1.2.1.1 Applications

IPL is to be cost/performance effective in support of timesharing, transaction, local and remote batch modes of business and scientific applications.

1.2.1.2 Compatibility

IPL is to be compatible across the range at the level of source language, data formats, recording media and the user interface. Instruction set compatibility is desirable but not mandatory. (See Section 4.1) Feature and capability subsetting may be practiced for certain system configurations.

1.2.1.3 Commonality

To reduce development, manufacturing and maintenance costs common elements are to be used across this line and from parent's predecessor lines. For example:

- Software product set
- Basic operating system
- I/O Subsystem, channels and controllers
- Peripheral devices
- Maintenance subsystems
- Implementation language

A major configuration design parameter is minimum life cycle cost.

1.2.1.4 Continuity

An incremental progression in processing power, system throughput and system capability is to be achieved through emphasis on hardware/software configurability, specialized scheduling algorithms and selective addition/deletion of software features.

1.2.1.5 Implementation Control

A broad range of applicability for the hardware/software products is to be assured through specification and use of engineering standards, software conventions and implementation

tools.

1.2.2 RELIABILITY/AVAILABILITY/SERVICEABILITY (RAS)

It is required to maximize time between interruptions, to continue operations in degraded mode and to minimize repair time/cost. Emphasis will be placed on hardware assists to RAS and software checking and recovery features. Hardware redundancy will be supported and may be required where RAS considerations dictate.

1.2.3 USABILITY

IPL will emphasize usability by the end user; application user or programmer.

For the application user, emphasis will be on the interface between the system and the user; defaults will be kept simple, consistent, and tutorial where necessary.

For the programmer, the emphasis will be on minimizing the total time between the coding and the correct execution of programs written in COBOL, FORTRAN and other languages. This will require:

- A balance between compilation speed and diagnostics to minimize both compilation time and the number of compilations.
- A capability to minimize the time to execute a single source language statement.
- Execution time support to monitor execution to aid debugging and re-implementation for improved performance.

Emphasis will be on remote access to the computing facility. Such access will encourage the development of applications through remote batch and timesharing terminals and encourage the use of the facility for transaction and timesharing applications. Program interface to the system will be compatible regardless of the mode of access; timesharing, transaction, batch or remote job entry.

1.2.4 MIGRATION

IPL is to support user transition from NCR's CENTURY and CRITERION and CDC's 3000L and CYBER lines to the extent that migration to IPL will be less costly and more desirable (RAS, usability, protection, storage structure) than converting to any other manufacturers product line.

1.2.5 PROTECTION/SECURITY

IPL is to supply a basic level of hardware/software protection which greatly exceeds predecessor machine lines. Sophisticated security and checking features are to be furnished as options.

1.2.6 STORAGE STRUCTURE

A storage structuring concept, virtual memory, will be utilized by IPL to meet the following product line objectives:

- Protection as noted above.
- Consistent management techniques for physical memories as their size grows over today's memories.
- Support for storage hierarchies and implicit I/O as technology allows.
- Improvement in operating system integrity.

2.0 REFERENCES

1) NCR/CDC Integrated Product Line Requirements and Goals; June 24, 1975.

2) Environments and Workloads Specification; June 13, 1975, ASL00315.

3) Reliability Test, Exponential Distribution (MIL-STD 781B); 11/15/67

4) Paper on "Availability" by P. G. Doran, 12/26/73.

3.0 CHARACTERISTICS AND FEATURES

3.1 CONFIGURATIONS

3.1.1 HARDWARE CONFIGURATIONS

3.1.1.1 Terminology

Terms to reference hardware elements:

Mainframe = processor(s) + main memory

Mainframe system = Mainframe + I/O subsystem(s)

Designators used to reference hardware elements:

Processor = Pn

Main memory = Mn

Mainframe system = Sn

where larger n indicates increased capacity and/or speed.

3.1.1.2 Mainframe Systems

An IPL mainframe system emphasizes configuration growth and connectability:

- 512Kd to 64MB main memory consisting of 1-4 integrated and/or stand-alone memory units;
  Each memory accessible by:
  - 1-4 central processing units, and
  - 1-8 I/O subsystems;
    each capable of handling:
    - special purpose local peripheral controllers(e.g., NCR common trunk, CYBER 170, 3000L)

- Integrated device controllers
- IPL channels, connectable to stations which may be controllers, (connectable to peripheral devices) or front end processors
- Handling 16 simultaneous streams.

3.1.1.3 Reconfigurability

Allow devices to be added to or dropped from a running system. Require specific device classes to run the system but not specific device models.

Provide facilities for incremental system expansion with minimum site disruption, system downtime and hardware returns.

3.1.1.4 Multimainframe

Support multiple mainframes through one or more of:

- Shared I/O devices.
- I/O channel connections (local or remote).
- Shared memory.

3.1.1.5 Component Capabilities

The Table below outlines the general classes and characteristics of system components to be supported in early IPL systems. See appendix B for a peripheral list.

COMPONENT	QUANTITY/MAINFRAME	CHARACTERISTICS
Terminals	1 - 4000	. 50 - 96K baud . Keyboard, CRT, special, Transaction, batch, data entry, multi-function
Front End	0 - 16	. Channel connection . Function oriented
Data Links	1 - 256	. 50 to 1.5M baud
Unit Record		
Card Readers	0 - 16	. 100 - 2000 CPM
Line Printers	0 - 16	. 100 - 3000 LPM
Card Punches	0 - 16	. 100 - 500 CPM
Paper Tape Readers	0 - 16	. 10 - 1000 CPS
Tape	0 - 64	. 200 - 6250 BPI . 10 - 200 IPS . 7/9 Track
Channels	1 - 32	. 500K-5M Bytes/Sec
Network Node	0 - 4	. Network Interface
Main Memory	512KB - 64MB	. 400 - 1000 NS Access
CPU	1 - 4	. .3 - 25 MIPS
Cache	0 - 128KB	. 20 - 100 NS Access
Mass Storage	140MB - 50000MB min 2 spindles	. 5 MS - 100 MS Access . 1 - 5 MB/Sec
Archival Storage	0 - 4X10**12B	. 1 - 10 SEC Access . 500K - 2 MB/Sec

3.1.2 SOFTWARE CONFIGURATIONS

3.1.2.1 Software Feature Configurability

IPL systems emphasize software feature tailoring:

- At the system level, major software features may be:
  - Basic to all systems
  - Optional, depending on user requirements
  - Separately packaged
- At the software feature level, component capabilities may be:
  - Minimum, to emphasize performance (subsetting)
  - Complete, for maximum capability
  - Alternative, to fit different environments (substitution)

The software configuration will include a performance base system supporting a limited number of features and feature options; and a feature base system supporting all feature options.

3.1.2.2 Reconfigurability

Allow substitution of most software components in a user running system environment to obtain different system performance and capability characteristics.

3.1.2.3 Local Communications

Develop common (local and remote) communication-oriented conventions for all page, line and transaction oriented I/O devices to allow maximum configuration flexibility.

3.1.2.4 I/O Control

Support I/O between external devices (staging) without the direct intervention of the CPU(s).

3.1.2.5 Networks

Support the network requirements of the parent companies. Direct definition of network systems is not to be undertaken by ASL. All design tradeoffs involving Networks will be based on CDC's Network Products specifications until NCR's are finalized.

3.1.2.6 Distributed Processes

Provide the capability to distribute selected system or user support processes to other processors connected to the mainframe memory directly or via channel (local or remote).

3.2 HARDWARE ELEMENTS

3.2.1 CENTRAL PROCESSOR (CPU)

Define a series of CPUs to support a range of performance and applications; specifically, capabilities for BDP, Scientific, Hardware-Emulation and language-virtual machine applications.

3.2.1.1 Instruction Set

Define instruction set(s) to handle the applications above. To include:

- linkage for switching control between IPL and virtual machines.
- BDP orientation, emphasizing code compaction in support of throughput.
- floating point orientation, emphasizing execution speed.
- memory management, emphasizing protection and large address spaces.

3.2.1.2 Virtual Machines

Support multiple virtual machines designed to use standard APLOS interfaces. Define virtual machines to support parent's predecessor systems (CENTURY, CRITERION, CYBER 170, 3000L), or new high level language virtual machines or other features.

3.2.1.3 Virtual Memory Mechanism

Define a virtual memory mechanism to support a large virtual address space by means of segmentation and/or paging. The mechanism is to include protection schemes for inter/intra process protection.

3.2.1.4 Other CPU Features

- External interrupts to/from other processors.
- Fast interrupt response time.
- Performance monitoring option.
- Process separation (protection) and memory interlocks.
- Procedure switching assistance
- Sensing to prevent error propagation

3.2.2 MAIN MEMORY

Memory objectives are:

- Span the product range at best cost performance. This implies:
  - Span range with fewest number of memory models.
  - Use cache memory in the CPU for performance differences with same memory model.
  - Lowest cost/bit including cache costs (memory volatility is acceptable).
- Maximize availability through:

  - Single Error Correction/Double Error Detection
  - Reconfigurability around failed memory element.
- Logical byte addressability

3.2.3 I/O CHANNELS

Provide the following capabilities with a single channel design:

- transfer rate/sec controller from main memory (being revised by joint NCR/CDC task force)
- attachable to at least 8 device controllers
- Contain error detection, recovery, and reporting mechanisms.
- Capable of being shared among 4 mainframe systems.
- Support high speed streaming.

3.2.4 DEVICE CONTROLLERS

- Dual channel access for control and/or data transfer.
- Up to 32 devices per storage controller.
- Storage controllers to permit multi block I/O as defined in section 7.2.2.2.
- Support multiple models of same device class.
- Maximum overlap of operation on separate device.
- Optionally support staging.
- Single functional design per device class.
- Each device controller design supports all channel speeds.

3.2.5 PERIPHERAL DEVICES

See Appendix B.

3.3 SOFTWARE ELEMENTS

3.3.1 OPERATING MODES

Support concurrent processing in any or all of the following operating modes in priority order for design trade offs:

- transaction
- time sharing
- remote batch
- local batch

All modes of operation must meet price performance requirements.

Design trade-offs between time sharing and transaction access modes may involve performance or security degradation. These cases will be specifically documented and approved by AD&C. When, in the judgment of AD&C, cumulative performance/security penalties to the time sharing or transaction mode exceeds "10%", the circumstances will be reported to the Planning Committee.

The system is to be capable of optimization for a specific operating mode. Do not specifically preclude implementation of a time-critical operating mode.

3.3.2 OPERATING SYSTEM

3.3.2.1 Broad Product Range

The operating system is the critical element in being able to span the broad range of performance, features and configurations of IPL. The objective is to span the range with a minimum number of OS variations.

3.3.2.2 Flexibility and Growth

The OS architecture, design and implementation must be maximally supportive and tolerant of future changes in market areas, application areas, technology and feature enhancements.

Provide a consistent interface to the operating system. Include the capabilities required for language compilers, system utilities, telecommunications, transactions, migration subsystems, application packages and user programs.

Do not provide special interfaces peculiar to the usage of any product set member which the product set member can provide itself. The intent is:

- to minimize the number of interfaces
- If a product set member demonstates a need for a previously unspecified interface, standardize and generalize the interface to make it available for other members.

3.3.2.3 Usability

Provide a consistent user interface between all modes of access (interactive, batch, operator communications; etc.) that is maximally supportive of a wide variety of users.

Accommodate single, multiple or remote operator console configurations utilizing standard I/O interfaces. Allow for generalized routing to specialized consoles. Minimize requirements for operator intervention. Design to execute in an unattended manner.

3.3.2.4 Integrity

Employ damage control mechanisms to detect, limit and correct the effects of system and/or job failures.

3.3.2.5 Features

Provide the basic services required to support:

- Physical and logical I/O

- Fail soft operation
- Operator communications
- Resource management and scheduling
- Usage accounting (user and vendor)
- System integrity
- Diagnostics and instrumentation
- Error detection, reporting and recovery
- Execution services
- Installation operations requirements
- Checkpoint/restart
- Concurrent maintenance

3.3.3 PRODUCT SET

The primary objective is to provide a single product set to span the entire IPL range without breaks in compatibility. Other common product set objectives include:

- All object code generated by IPL compilers to be sharable (in support of reentrant applications).
- Maximize the use of common design, common code modules and common libraries.
- A common IPL product set interface standard to achieve:
  - Object code communication across the product set (e.g., a COBOL program can call a FORTRAN subroutine).
  - Common object text format to facilitate the linking of object programs produced by two or more compilers.
  - Record and file formats will be common and interchangeable across the product set.
  - There will be one or more data representations common across the product set.
- Provide compatible external user interfaces to all similar IPL product set members.
  - A compatible means for invoking all compilers.
  - Compatible graphic output formats from all compilers.

  - Compatible diagnostic messages for all compilers.
- Provide statistical, performance and system debugging hooks and tools for both system and user level use.
- For products covered by standards in Appendix C, provide options to flag, accept and/or reject all non-standard statements.
- All compilers will allow:
  - Initiating a batch compilation by an interactive user.
  - Interactive communications with a terminal during execution of user programs.

3.3.3.1 Design Objectives/Priorities

	PRODUCT TRADE-OFFS: COMPATIBILITY	FEATURE RICHNESS	REAL MEMORY USE	COMPILE SPEED	EXECUTION SPEED	TEST BASE SIZE	CODE COMPACTION	COMPATIBILITY PRIORITY: CRITERION	CYBER	ANSI	3000L	IBM		REMARKS
APL	1		2		3				2			1		IBM APL TARGET
BASIC			1	2						1				BATCH AND INCREMENTAL
COBOL								2	3	1				ANSI 74 (HIGH LEVEL
PRODUCTION			3		2		1							MEASURED BY NAVY AUDIT)
DEVELOPMENT			1	2	3									
FORTRAN														ANSI 75 (HIGH LEVEL)
PRODUCTION	2				1	3			1	2				
DEVELOPMENT	3		1	2					1	2				
PL1	2					1			1	2		3		
SHL														CYBER ISHL CC COMPATIBLE
PRODUCTION				3	2		1		1					
DEVELOPMENT			2	1					1					
SORT/MERGE														PRODUCT SET PROGRAM CALL
CYBER FE	3		2		1				1	2				CYBER CONTROL STATEMENTS
CRITERION	3		2		1			1		2				CRITERION CTRL STATEMENT

FE = FRONT END

3.3.3.2 Utilities to be Supplied

PROGRAM ORIENTED	Source code maintenance Object code maintenance Line and text editor Text formatter Debugging aids

DATA ORIENTED	General utilities
	  Copy (housekeep)
	  Compare
	  Reformat
	Data base
	  Subset extractor
	  Boolean processor
	  Index management
	  Restructure/reorganization
	  Usage analysis
	  Log/audit
	  Recover/restore

MEDIA ORIENTED	Initialization Dump/restore

SYSTEM ORIENTED	Maintenance log analysis
	System use log analysis
	Dump/load job queue
	System generation/modification
	Terminal use
	  System/job/file status
	  Message capability
	Permanent files
	  Dump/load
	  Audit
	General file utilities
	Print memory or file

CONVERSION AIDS	Data conversion Program conversion

Where applicable, utilities will meet compatibility constraints as outlined in section 3.3.3.

3.3.4 DATA BASE MANAGEMENT (DBM)

The primary objective of the DBM system is to span the IPL range with a secure data base management facility that is compatible across the line. The long term objective is to produce an ANSI-compliant DBM system.

The utilities and common product set objectives specified above apply to the DBM system.

3.3.4.1 Evolutionary Growth

Accommodate the need for subset product delivery and pricing. The basic system must contain the key elements and features of a DBM product; storage and data independence, protection, etc.

3.3.4.2 Foreign Systems

Provide the user the alternative to use a foreign data base management system (TOTAL)in lieu of the IPL DBM system. Foreign and IPL DBM systems are not required to share data bases but should be capable of sharing physical resources.

3.3.4.3 Design Trade-Off Priority

Within the constraints of balanced product set performance objectives, the design trade-off priorities are:

- Run time efficiency over storage requirement.
- Storage requirement over compilation or utility efficiency.
- Retrieval over update performance.
- Modify over store over delete performance.
- Compatibility deviations from the DMS170 and CODASYL designs will be specifically documented and approved by ADSC and made visible to the Planning Committee.

3.3.4.4 Data Access

Access to the data base to be available through COBOL, FORTRAN, and Query Update as well as through direct user interface in both a batch and interactive mode.

Data Description and Data Manipulation languages in a form familiar to applications programmers.

File organizations adaptable to massive insertions and deletions.

Access can be inuependent of the organization and format of the data base. Access methods available to the user include sequential, direct (by symbolic key, e.g., index sequential) and associative (value coupled sets).

3.3.4.5 Data Integrity

Maintain accurate records of supporting indexes and file structures, etc., to insure that purged or unused files are properly designated.

Prevent propagation of detectable hardware failures in the data base.

Concurrent updates from multiple tasks or applications not to result in a breach of integrity.

Provide optional audit trails and tracking of all accesses.

3.3.4.6 Program Independence

Allow programs to be maximally independent of:

- Medium and device type
- Volume residency
- Storage structure
- Storage format
- Storage address

3.3.4.7 Query/Update

A basic terminal oriented QUERY and UPDATE language.

3.4 SECURITY

As many security features as possible will be optional to the user or computer manager to reduce system overhead when desired.

The objectives of the IPL security system are to provide:

- Mechanisms to identify each user attempting to use the system; to set authorization, classification and privilege levels for each user; to limit a user's access to and usage of system resources and data files; to audit activities in the system.
- Mechanisms to identify terminals and peripheral devices attached to the system.
- Detection, reporting and logging of security violations. Alarm generation when security violations are detected.
- Data access and usage regulated by the owner of data; data transmission according to limits set by the owner of the data; clearing of residual classified data.
- Security safeguards for startups, shutdowns, restarts and system modification.

Additionally, the following goals will be pursued to the limits imposed by other architectural, design, and implementation considerations:

- the least possible amount of privilege granted to operating system functions.
- Internal and external labeling of classified information.
- Establish an operating system security model and continually test the OS design and implementation.

3.5 PROTECTION

The overall protection objectives for IPL are to protect the user from other users, the system from users, users from the system, and system elements from other system elements.

Data can be protected at the:

- File level
- Record level
- Element level (through DBM)

3.6 MIGRATION

Systems to be addressed for migration include specific versions of:

- 3000L/MASTER
- CYBER/NOS, NOS/BE (including I/O emulation)
- TOX application programs
- CRITERION/B1-B2-VRX but not CVM (only requires emulation of B1-B2 OS code)

3.6.1 HARDWARE MIGRATION

The IPL will support a hardware migration environment with:

- Emulation of the CYBER 170, 3000L, CENTURY and CRITERION Central processors.
- Support of selected peripherals available on the CYBER, 3000L and CRITERION lines in their current mode.

3.6.2 CPU PROGRAM MIGRATION

The IPL will support program migration with:

- Emulation to permit execution of old mode programs directly without change or recompilation.
- Recompilation and/or utilities for converting old programs to IPL mode.

It is highly desirable that parent companies prepare for migration from existing lines to IPL (compatible compiler languages, command languages, data formats and media).

3.6.3 DATA MIGRATION

Data Migration will be accommodated with:

- Utilities that convert old files to the IPL formats and/or media. Such conversion will be explicitly reversible.
- Support old files for access by programs executing in old or new mode according to the chart below. The numbers represent the preferred sequence of migration steps.

	FILES		
	OLD STRUCTURE		IPL STRUCTURE
PROGRAMS	IPL SUPPORTED OLD DEVICE MODE	IPL DEVICE	IPL DEVICE
EMULATION MODE	1	(1a)	
IPL MODE	2	(2a)	3

Note: For step 2 the objective is to support a subset of old structures. Steps (1a) and (2a) are not design objectives but represent alternatives pending resolution of parent peripheral strategies.

An IPL device is one which supports IPL data structures in its native mode. "IPL Devices" are specifically listed in APPENDIX B.

4.0 COMPATIBILITY OBJECTIVES

4.1 WITHIN IPL

The IPL will present a compatible data interface that is accomodated across the line. This objective includes provisions for:

- Compatible instructions will have identical results.
- ANSI standard data representation on cards and tape.
- IPL standard data formats (internal and external).
- IPL standard disk recording formats (physical and logical file level) for each transportable media type.
- IPL standard operating system interface.

The IPL standard data formats are:

- 8-bit bytes.
- Internal representation of character data in ASCII.
- 32 and 64-bit representation of fixed point numbers.
- 64 (single precision) and 128-bit (double precision) representation of floating point numbers.
- Signed and unsigned packed decimal numbers.
- Signed (embedded and separate/leading and trailing) and unsigned zoned decimal numbers.
- Address pointers and synchronization elements.

4.2 PARENT PREDECESSOR PRODUCTS

Any preliminary systems which are based on CRITERION or 6150 hardware elements must be field upgradable to IPL systems at a minimum cost. For NCR systems, user reversibility is required.

The results of the IPL floating point operations will be arithmetically compatible to the normal range of CYBER 170 floating point unrounded results.

Where feasible, use software products implemented in a higher level language only. Evolve the product to IPL specifications on the predecessor system. Candidates include:

- Compiler products
- Data management products
- Network products

4.3 COMPANION PRODUCTS

IPL peripherals will normally be supplied by CPI and MPI.

4.4 COMPETITIVE PRODUCTS

MEDIA INTERCHANGE

Device	Vendor	Physical Recording	Conversion Code	Logical Structuring
7 Track tape	-	ANSI 200bpi NRZI (read only) 556bpi NRZI 800bpi NRZI	BCD (even parity)	o ANSI 1968 and 1976
9 track tape	-	ANSI 800cpi NRZI 1600cpi PE 6250cpi GCR	ASCII EBCDIC	o ANSI 1968 and 1976
80 column cards	-	ANSI	ASCII 029 026 Transparent	o Card Image
Diskette	IBM	IBM 3750 format	EBCDIC	o Unit Record

Secondary support of EBCDIC character and decimal data by CCBCL programs will be provided to the extent EBCDIC media are supported above.

5.0 SYSTEM ENGINEERING CONCEPTS

5.1 SYSTEM DESIGN

Techniques of design and implementation (e.g., structured design, data coupled interfaces) are to be employed which will allow a new level of functional isolation. This will present the parent companies with the opportunities listed below as well as the challenge of improving integration, distribution and field maintenance enough to profit from this modularity.

5.1.1 FLEXIBLE PACKAGING OF SYSTEM COMPONENTS

To permit:

- replacement of system components to gain new functionality without disruption.
- identical functions for both small and large system users with reductions in performance rather than function. However, a meaningful subset of functions may be required to support minimum level systems.
- customer growth.
- system adaptability to unique environments.
- system optimization to satisfy specific performance requirements.

5.2 IMPLEMENTATION LANGUAGE

Define and use a common software writers language (SWL) for the entire product line development. This is expected to:

- Reduce development and support costs
- Enhance probability of the system software spanning the entire product line
- Allow definition of hardware/firmware assists which improve SWL code performance and thus the whole system performance.
- Enhance RAS
- Facilitate transportation of algorithms, programmer expertise and (to a lesser extent) software with other machine lines.

5.3 STANDARDS

The IPL systems will comply with all applicable NCR-CDC joint and industry standards. Any deviations will be identified with waiver statements in future design documents. See Appendix C for full standards list.

6.0 PRODUCT PHASING OBJECTIVES

A design objective is that phased implementation and release of selected features, functions, and components can be conveniently accommodated.

The content of the first release and proposed subsequent phases will be delineated in the Architectural Definition Document by 1/15/77.

Features and components to be considered for phased inclusion in IPL systems are:

- Modes of operation and the associated scheduling and system tuning capabilities.
- Optional levels of security.
- Multimainframe support.
- Utilization of hardware protection mechanisms
- Command Language features associated with modes of operation.
- Data Base Management features.
- File management capabilities in support of phased DBM features.
- Support for a storage hierarchy (tape library, bulk memory, etc.).
- RAS features such as file archiving and automatic hierarchy management.
- Diagnostics may be phased from on-line fault detection to fault isolation without a retraining requirement.
- General features of the product set members depending on the phasing of modes of operation and configurations. Examples are on-line debugging and performance optimizing compilers.

- Peripheral support.
- Virtual language processor support.
- Where language standards are defined, initial design will give predecessor product compliance priority over full compliance.

7.0 PERFORMANCE OBJECTIVES

The IPL Architecture must allow the largest cost/performance range possible between the smallest model and the largest model. The range must be covered continuously with no cost and/or performance gaps within the line.

Identifiable computer models must occur at performance level ratios of 2.5 to 3.5. At each model level, a minimum starter system must be configurable with growth through add-on and/or replacement of hardware modules to allow the user to install a system at the lowest possible cost, and to grow in smaller steps than with total system replacement.

The IPL systems should minimize the total time between the coding and correct execution of a program. Approaches to be considered include:

- Emphasis on compilation speed
- Emphasis on diagnosis
- Independent module generations and execution
- Debug aids

The IPL processors of higher cost and performance must be efficient in the execution of FORTRAN and those of lower cost and performance must efficiently support COBOL.

7.1 SYSTEM COST/PERFORMANCE GOALS

See Appendix E

7.2 COMPONENT PERFORMANCE OBJECTIVES

7.2.1 PRODUCT SET

7.2.1.1 Performance Levels

Major language processors are to provide for two levels of compilation performance.

- Development mode, characterized by extensive diagnostics and fast compilation rate at the expense of object code efficiency.
- Production mode, characterized by highly efficient object code (space/speed) generated at the expense of compilation rates.

PRELIMINARY
PRODUCT SET PERFORMANCE OBJECTIVES
(SUBJECT TO FURTHER REVIEW WITH PARENTS)

PRODUCT	WORKING SET SIZE* KB	STATEMENTS PER MINUTE COMPILE RATES		TOTAL CODE SPACE KB
		P2 CPU ***	WALL CLOCK**	
APL	100KB	20,000	6,000	300KB
BASIC				
INTA	100KB	20,000	6,000	200KB
PROD	100KB	10,000	2,500	500KB
COBOL				
PROD	130KB	4,000	1,000	1.5MB
	65KB	TBF	TBF	
DEV	120KB	8,000	3,000	
FORTRAN				
PROD	150KB	7,000	1,000	750KB
DEV	125KB	13,000	5,000	250KB
PL1	150KB	2,500	350	1.5MB
S/MERGE	TBF	TBF	TBF	TBF
QU	TBF	TBF	TBF	TBF
DDL	TBF	TBF	TBF	TBF
DBMS	TBF	TBF	TBF	TBF
SAL				
PROD	200KB	4,000	1,350	TBF
DEV	150KB	10,000	3,400	TBF

* "TYPICAL" PROGRAM >500 DATA NAMES, >1000 STATEMENTS
** UNLIMITED REAL MEMORY (NO MORE THAN 10% DEGRADATION AT WORKING SET SIZE)
*** RELATIVE PERFORMANCE RATIOS THAT APPLY TO OTHER PROCESSORS ARE DESCRIBED IN SECTION 7.2.3.3.
TBF - To be supplied with Architectural Definition

7.2.2 SYSTEM PERFORMANCE

7.2.2.1 Monitoring/Tuning

Provide mechanisms supporting measuring of operating system and general software performance and usage characteristics. Supply basic analysis tools for presenting this data in meaningful terms. Self measurement tools and services to be optionally selected.

Support system tuning at system generation, system load and execution times. Include tuning options to maximize performance in the following areas:

- time sharing
- transaction
- batch, local/remote

The level of performance achievable in any particular area is not required to be at the level of specifically developed dedicated application systems but the standard IPL OS must be able to supply the majority of code that would make up such dedicated special systems.

7.2.2.2 Data Transfers

Each I/O subsystem will be expandable to sustain up to a 20MB data rate. Each must permit simultaneous operation of up to 16 device controllers. The IOSS will not inhibit controllers from driving devices at rated speeds (within overall IOSS bandwidth limits.)

I/O protocol must not preclude transfer rates of 64 megabytes per second when appropriate technologies are available.

The IPL must support a highly efficient I/O capability in multiprogramming or monoprogramming modes.

Burst data transfer rates at device maximum

Effective data transfer rates at 80% of device rated speed.

Support data streaming. Streaming (multi-block I/O) is the ability to process two or more consecutive I/O requests for the same device without degrading the effective transfer rate. The number of simultaneous user data streams is configuration

dependent. Extra controller costs (if any) to meet this requirement will be identified.

7.2.2.3 CS Workloads

The following workloads must be able to run on a minimum configuration:

- Dedicated Batch Mode - Minimum of 3 concurrent jobs (1 compilation and 2 production jobs, BDP oriented)
- On-line/Batch Mode - One on-line job with up to 35 terminals, mixed types, transaction oriented, with a throughput of 3 to 4 transactions per second. (For measurement purposes, a transaction is an externally generated INPUT/PROCESS/OUTPUT sequence requiring no more than 6 to 8 accesses to RMS during processing.) Two batch jobs (1 compilation and 1 production job, BDP oriented).
- Dedicated On-line Mode - One on-line job with up to 100 terminals, mixed types, transaction oriented, with a throughput of 6 transactions per second.

7.2.3 PROCESSOR PERFORMANCE

PROCESSOR PERFORMANCE IS NOT TO BE CONSTRUED AS SYSTEM THROUGHPUT.

The performance objectives for processors are listed in the following sub-paragraphs. The stated performance objectives will be met with the following conditions imposed:

- No conflicts in main memory from other processors.
- Main memory access time (including cables) of 1008 nsec.
- Cache hit rate is C as defined below. This means that (1-C) of the words to be read from main memory, excluding instruction references, shall not be in the cache and shall require a reference to main memory.
- Map hit rate of M as defined below. This means that (1-M) of the process virtual address to real memory address translations shall require a reference to main memory for access to segment or page table information.

PROCESSOR	CACHE HIT RATE (C)	MAP HIT RATE (M)
P1		90%
P2	75%	98%
P3	75%	99%
P4	90%	99.5%

7.2.3.1 Scientific Performance Objectives

P1 Processor - 0.75 x CDC CYBER 70/73
P2 Processor - 3.0 x CDC CYBER 70/73
P3 Processor - 9.0 x CDC CYBER 70/73
P4 Processor - 27.0 x CDC CYBER 70/73

Compliance with these objectives will be determined by the execution time of the ten FORTRAN kernels listed in the Environments and Workloads Specification.

7.2.3.2 Business Performance Objectives

P1 Processor - 2.3 x IBM 370/145
P2 Processor - 7.3 x IBM 370/145
P3 Processor - 18 x IBM 370/145
P4 Processor - 40 x IBM 370/145

Compliance with these objectives will be determined by the execution time of the COBOL S-PROFILE statements listed in the Environments and Workloads Specification.

7.2.3.3 Software Writer Language Performance Objectives

P1 Processor - 1.0 x CDC CYBER 70/73
P2 Processor - 2.7 x CDC CYBER 70/73
P3 Processor - 7.3 x CDC CYBER 70/73
P4 Processor - 19.7 x CDC CYBER 70/73

Compliance with these objectives will be determined by the execution time of the SWL PROFILE kernels listed in the Environments and Workloads Specification.

8.0 RELIABILITY OBJECTIVES

8.1 SYSTEM MEAN TIME BETWEEN FAILURE (MTBF)

A system failure means that a fault has occurred which prevents the system from producing any acceptable work. Human intervention is required to return the system to an operational state.

Mean time between system failures (System MTBF) is defined as the mean time between the start of successive system failures. This mean time includes operational time and all system down time resulting from a failure, including the mean recovery time required to store the system to its original state. All MTBF's are stated in hours.

8.1.1 SYSTEM OBJECTIVES

The objectives for the System MTBF for systems S0-S4 are shown below. The objectives are specified at release and during two periods after release. Release objectives shall be measured by Test Plan IV of MIL-STD-781B, 11-15-67. Release is the first shipment to a paying customer.

System	At Release	Mean During First 12 Months	Mean During Third Year
S0	100	150	400
S1	100	150	375
S2	95	140	320
S3	100	150	385
S4	95	130	340

These objectives are based on the inherent hardware system MTBF's as estimated by mathematical modeling techniques. The

curves in Appendix F have been included for reference.

8.1.2 HARDWARE MTBF OBJECTIVES

The hardware components of the system MTBF objectives are tabulated below. The figures in parentheses are the mathematically calculated MTBF's based on 30%, 40% and 55% of inherent MTBF for S0-S2 and 22.5%, 30% and 55% for S3-S4; they are included for information only.

System	At Release	Mean During First 12 Months	Mean During Third Year
S0	300 (310)	350 (370)	660 (570)
S1	300 (250)	350 (330)	600 (450)
S2	250 (180)	300 (250)	500 (340)
S3	300 (330)	400 (450)	750 (740)
S4	250 (220)	325 (280)	650 (530)

8.1.3 SOFTWARE MTBF OBJECTIVES

The operating system components of system MTBF objectives are tabulated below. These are estimates based on the following assumptions:

- MTBF is measured in a user environment, not by development stress-testing.
- The same basic software system is used throughout, with only validated bug fixes added.
- There is no radical change in the nature of the user's production workload.

The figures in parentheses are estimates of the system's MTBF in a development test environment. The third year figures are omitted because feature enhancement is the expected mode of system evolution.

8.0 RELIABILITY OBJECTIVES
8.1.3 SOFTWARE MTBF OBJECTIVES

System	At Release	Release + 1 Yr.	Mean During Third Year
S0	150 (112.5)	262 (250)	1000
S1	150 (112.5)	262 (250)	1000
S2	150 (112.5)	262 (230)	900
S3	150 (112.5)	240 (210)	800
S4	150 (112.5)	225 (175)	700

These figures represent objectives for a performance O.S. variant. Full feature variant not to degrade more than 10%.

8.2 AVAILABILITY

8.2.1 SYSTEM AVAILABILITY

$$1 = \text{Mean Time Between System Failures} \;/\; \text{Mean Down Time}$$

where:

- Mean Down Time = Mean Time to Repair (MTTR) + Mean Time to Recover + Mean Wait Time + Preventive Maintenance (PM).
- Mean Time to Recover is the mean re-run time necessary to return the system to its original state and the jobs it was executing to their original state.
- Mean Wait Time is the mean time it takes for an engineer to be made available to address the fault. With the exception of software faults this time estimated as one hour.
- Preventive Maintenance is any scheduled maintenance where concurrent maintenance is assumed to reduce system availability by the amount of system resource required.

Objectives for System Availability for systems S0-S4 are shown

8.0 RELIABILITY OBJECTIVES
8.2.1 SYSTEM AVAILABILITY

below. The time periods are those used for the System MTBF objectives.

At Release	Mean During First 12 Months	Mean During Third Year
.96	.965	.97 (including PM)
.975	.98	.985 (excluding PM)

Note: Definitions in this section have been drawn from the paper entitled "Availability" by P. G. Doran, 12/26/73.

8.2.2 ACCEPTANCE AVAILABILITY

When a system is undergoing acceptance testing, availability is defined using different assumptions:

- Mean Wait Time is zero, the system is attended.
- Preventive Maintenance is not included in Mean Down Time.
- Software MTBF approximates that of development test rather than user environment (see Section 8.1.3).

Objectives for Acceptance Availability for systems S0-S4 are shown below. They apply to discrete times rather than intervals.

At Release	Release + 1 Yr.	Release + 3 Yrs.
.98	.985	.99

8.3 RAS FEATURES

The guidelines for total costs for RAS features for a given system will be 15% of hardware MLB and 33% performance impact on O.S. software (both within cost/performance objectives).

8.3.1 RELIABILITY

The scope of reliability is to reduce failure rates of hardware and software, and minimize component faults from becoming element and system failures. Specifically, reliability is defined as preventing the occurrence or propagation of errors. Reliability features should include:

- Parity checking on major data paths, address paths, channels, registers and memories.
- Error status registers.
- Time-out mechanisms to provide continuous operation of system facilities.
- A validation check of disk write positioning.
- Checksum techniques for key system tables.
- The deadstart process to include confidence level tests run against critical system components.
- Methods of forcing conditions so that checks can be made of the reliability circuitry.

8.3.2 AVAILABILITY

Availability is defined as providing alternate paths around failing or failed system functional components to minimize impact on a running production system. Availability features should include:

- Capability to "fault" portions of the cache buffer and map buffer.
- The presence of another processor on systems to ensure recovery from a failed CPU.
- SEC/DED implemented on main memory.
- A combination of hardware and software techniques to be used to retry failing instruction setup.
- Execution of user supplied recovery algorithms after

standard system error recovery procedures.

- Reconfiguration by a combination of hardware and software techniques following failures, automated as far as possible.
- Use of motor generator sets as a customer option to decrease sensitivity to commercial power.
- Recovery facilities both at the individual job and at the system level, such that the environment may be re-established after a system failure.

8.3.3 SERVICEABILITY

Serviceability is defined as the effectiveness of error isolation and maintenance support. Serviceability features should include:

- Error signals which localize faults.
- Micro-program control of instruction execution.
- Minimize the number of module types with all like modules fully interchangeable and replaceable when power is on.
- Design IPL Maintenance Services to allow hardware maintenance to be performed concurrent with customer operation.
- A maintenance panel to provide the following capabilities:
  - System master clear button
  - System deadstart button
  - Fault indicator
  - Power fault indicator
  - Cooling fault indicator
  - Programmable audio alarm
- Not to require a dedicated maintenance console.
- Allow an input/output device to be completely dedicated to maintenance usage for initial micro code load, micro diagnostics, micro dumps, etc.
- Privileged operational modes to allow the maintenance service facilities, under program control, to vary

margins.

- Logging of transient and permanent faults. Logging of deadstart recovery conditions.

- A systematic set of diagnostics aimed at isolating 95% of the faults to three or less replaceable modules and 90% to one module.

- Relinquish all but a minimum of system components to concurrent on-line maintenance as needed. Relinquish remaining components to dedicated on-line maintenance without losing "system state".

- Remote access to those facilities under O.S. control which can be used for routine hardware and software maintenance.

9.0 PROGRAM ASSUMPTIONS

9.1 SYSTEMS PROJECTION

SYSTEM MODELS	S0	S1	S2	S3	S4
Auerbach Lease Range Category	$5-18K	$13-37K	$25-51K	$44-88K	$76-152K
First Customer Shipment	1Q80	4Q79	1Q80	1H81	2H82
Last forecasted Shipment	2H84	1H85	2H88	2H89	1H90
Number of Systems	680	400	325	180	60

9.2 CONSTRAINTS

Constraints imposed on the IPL program include:

- Interface to CDC and NCR networks.

- Use of existing NCR-CRITERION hardware for initial versions of the S0, S1 and I/O subsystem. Components include:

  CRITERION Processor
  ITB
  DMA-MUX
  Integrated Communications Adapter
  Integrated Disk Controller
  Integrated Memory

  Objectives dependent on P1 and IOSS are affected by this constraint. In particular, all mainframe elements are

constrained to be synchronous to a 56 nsec clock.

- Use of existing software design, interfaces and products including:

  CDC STAR COBOL/NCR VRX COBOL
  CDC FORTRAN 5
  CDC QUERY/UPDATE

- Use of CENTURY diagnostics for maintenance of CENTURY peripherals (initial IPL configurations).

- Must regularly provide design information to standalone emulation projects using IPL components.

10.0 OBJECTIVES UNDER CONSIDERATION

10.1 SOFTWARE PRODUCTS

APL and PL/1 are not planned for the initial IPL Product Set offering.

Dynamic automatic memory reconfigurability for fail soft recovery.

Remote operator system initialization.

DBMS Data Access from PL1

10.2 HARDWARE PRODUCTS

The following main memory products are being actively considered for IPL systems:

M0A - Same general capabilities as M0 with a capacity of 2MB to 8MB.

M2A - Same general capabilities as M2 with a capacity of 4MB to 16MB.

M3A - Same general capabilities as M3 with a capacity of 16MB to 32MB.

A P5/M5 system may be required in later IPL systems.

CYBER 170 PPU hardware emulation.

10.3 COMPONENT RELEASES

Functional component releases in binary or source form must be provided with the attendant capability of a user to augment his system with the component without a complete system generation.

10.0 OBJECTIVES UNDER CONSIDERATION
13.3 COMPONENT RELEASES

As a result of functional releases, the system will contain a variety of components at various release levels. Maintenance practices must be revised in accordance with this new environment.

11.0 OBJECTIVES OF LOWEST PRIORITY

11.0 OBJECTIVES OF LOWEST PRIORITY

- Interface to IBM System Network Architecture unless an integral part of parent's network architecture.
- Emulation of IBM 370 processors.
- Compatibility with existing parent's operator to O.S. interfaces.
- ALGOL and RPG, which have been standard offerings of one or both of the parents prior product lines, are to be excluded from the IPL Product Set.
- 256K bytes of central memory as a minimum memory configuration requirement.
- Emulation of NCR language virtual machines.
- Full DOD security compliance.

12.0 APPENDICES

The appendices represent the most recent development objectives of the program. The data in these appendices is subject to revision, review and approval independent of the full Architectural Objectives document.

12.1 APPENDIX A - COST OBJECTIVES

12.1.1 DEVELOPMENT COST OBJECTIVES

See IPL Program Plan

12.1.2 INSTALLATION AND MAINTENANCE COST OBJECTIVES

12.1.2.1 Hardware

Emphasis will be placed on ease of installation including parameters such as:

1) Physical interconnectability
2) Environmental requirements

to the end of reducing installation costs.

The monthly maintenance cost incurred by the supporting field service organization must not exceed the following levels (expressed as a percentage of MLB) for IPL mainframe elements (peripheral equipment excluded):

Mainframe System Model	Life Cycle Average Monthly Maintenance Cost	Second Year Monthly Maintenance Cost Objective
S0	.9%	.9%
S1	.8%	.8%
S2	.65%	.7%
S3	.5%	.6%
S4	.4%	.5%

These costs are defined to include both the direct cost of maintaining the equipment and the allocation of various indirect costs, as follows:

Direct Cost

Direct Costs include the following labor, travel and parts category:

- Remedial Maintenance Labor
- Preventive Maintenance Labor
- Associated Repair Labor
- Consumable Parts
- Rework of Replaceable Modules
- Travel Time and Expenses (for field service personnel)

Indirect Cost

Indirect costs include the allocation of the following expense categories:

- Training (for field service personnel)
- Tools and Test Equipment
- Spare Parts Inventory
- Diagnostic Software Maintenance and Distribution
- Field Retrofits (field/engineering change orders)
- Home Office Support

12.1.2.2 Software

Installability features will emphasize:

1) Simple field O.S. installation secuence

2) Automated or semi automated configuration definition.

to the end of reducing installation costs.

The estimates below reflect software maintenance costs for the first 5-years following release. These estimates are based on the following assumptions:

	S0-S1 CLASS		S2-S4 CLASS	
	NCR EXP.	IPL EST.	CDC EXP.	IPL EST.
Cost to fix one bug	$1100	$500	$675	$500
Bugs per customer month - 1st year	na	1	na	2
- following	.5	.5	2	1

SOFTWARE MAINTENANCE COSTS

YEAR	1980	1981	1982	1983	1984
Number systems shipped					
S0-S1	240	250	240	210	100
S2-S4	25	70	95	90	75
"maintenance" cost in millions	$1.8	$3.2	$4.7	$5.7	$6.0

12.2 APPENDIX B - PERIPHERALS

- To be updated in accordance with CDC/NCR peripheral device support task force -

12.3 APPENDIX C - STANDARDS

IPL systems will comply with the following standards. The objective is to be fully compliant. Deviation waivers will be requested on a product by product basis.

Title	JNT or Industry No.	NCR No.	CDC No.	Compliance Planned: Applicable Standard	Compliance Planned: Option Selected
Category - CODES					
Code for Information Interchange	X3.4-1968				
Holerith Punched Card Code	X3.26-1970				
Implementation of the Code for Information Interchange and Related Media Standards	FIPS PUB 7				
Subsets of the Standard Code for Information Interchange	FIPS PUB 15		1.10.003		
6 and 7 Bit Coded Character Sets for Information Processing Interchange	ISO 646-1973				
Code Extension Techniques for Use with the ISO 7-Bit Coded Character Set	ISO 2022-1973				
Graphic Representation for the Control Characters of the ECMA 7-Bit Coded Character Set for Information Interchange	ECMA 17-1968				
Alphanumeric Character Set for 7x9 Matrix Printers	ECMA 42-1973				
Category - REELED MAGNETIC TAPE MEDIA					
Recorded Magnetic Tape for Information Interchange (200 CPI, NRZI)	X3.14-1972		1.10.013		
Recorded Magnetic Tape for Information Interchange (800 CPI, NRZI)	X3.22-1973		1.10.005		
Recorded Magnetic Tape for Information Interchange (1600 CPI, Phase Coded)	X3.39-1973		1.10.006		

Title	JNT or Industry No.	NCR No.	CDC No.	Compliance Planned	
				Applicable Standard	Option Selected
Category - PROGRAMMING LANGUAGES					
COBOL	X3.23-1974				
Common Business Oriented Language (COBOL)	FIPS PUB 21-1				
FORTRAN	X3.9-1976				
Basic FORTRAN	X3.10-1976				
Category - SPECIAL PURPOSE LANGUAGES					
Industrial Computer System Fortran Procedures for Executive Functions and Process Input-Output	ISA S61-1-1972				
Category - OPERATING SYSTEMS					
Magnetic Tape Labels for Information Interchange	X3.27-1975		1.87.002		
Magnetic Tape Error Detection and Recovery			1.87.004		
System Error Recovery for Rotating Mass Storage			1.87.005		
Category - DATA REPRESENTATION					
Representation for Calendar Date and Ordinal Date for Information Interchange	X3.30-1971				
Category - DATA COMMUNICATION					
Standard Data Communication Channel Control Procedures for ASCII			1.10.002		
Use of Longitudinal Parity to Detect Errors in Information Messages	ISO 1155-1973				

Title	JNT or Industry No.	NCR No.	CDC No.	Compliance Planned: Applicable Standard	Compliance Planned: Option Selected	
Basic Mode Control Procedures - Conversational Information Message Transfer	ISO 2629-1973					
Code Independent Information Transfer	ECMA 24-1969					
High-Level Data Link Control Procedures (HDLC) - Frame Structure	*ISO 3309.2-1975					
SDLC Communication Protocol		7-04-01				
Category - ENVIRONMENTAL						
Application Guidelines			1.03.201			
Temperature, Humidity and Barometric Pressure .Temperature, Humidity .Pressure	JNT-STD 31-01	2-11-01	1.03.202			
Applied Voltage and Frequency Ranges .Voltage .Frequency .Transients		2-11-02	1.03.207			
EMI/RFI (Emission)	JNT-STD 31-03	2-11-08	1.30.022			
Acoustical Noise	*JNT-STD 31-04	*2-10-02	1.20.007			
Vibration and Shock Design Criteria	*JNT-STD 31-05	*2-11-03	1.03.203			
Vibration and Shock Packaging Criteria	*JNT-STD 31-10		1.03.203			
Air Cleanliness	JNT-STD 31-06		1.03.205			
Visual Displays	JNT-STD 31-07	*2-11-04	1.03.206			
EMI/RFI (Susceptibility)	JNT-STD 31-08	2-11-09	1.30.022			
Physical Characteristics	JNT-STD 31-09		1.03.209			
Test Code for the Measurement of the Airborne Noise Emitted by Rotating Electrical Machinery	ISO R1680-1970					

Title	JNT or Industry No.	NCR No.	CDC No.	Compliance Practice: Applicable Standard	Compliance Practice: Option Selected
tegory - GENERAL DESIGN					
mponent Selection			1.03.002		
mponent Qualification			1.03.003		
Microcircuit Qualification	JNT-STD 30-01				
ectronic Logic Packaging			1.03.006		
crocircuit Procurement and Acceptance Test ecifications			1.03.007		
ecifications for Finishing Vendors Handbook			1.03.100		
oduct Safety, Design and Certification	JNT-STD 35-01	3-02-11	1.30.003		
tegory - MECHANICAL DESIGN					
erating and Maintenance Meters			1.20.008		
dustrial Design			1.20.010		
ysical Units and Comparisons			1.20.031		
tegory - ELECTRICAL DESIGN					
neral Design Standard for Electronic Power pplies			1.30.001		
fety Color Coding of Flexible Cords	JNT-STD 35-02		1.30.005		
lor Coding of Wires, Harnesses and Cables			1.30.005		

Title	JNT or Industry No.	NCR No.	CDC No.	Compliance Planned: Applicable Standard	Compliance Planned: Option Selected
Cable Classification and Marking			1.30.008		
Computer and Peripheral Equipment Design Requirements			1.30.011		
Electromagnetic Compatibility Design Guide Handbook			1.30.020		
Computer Grounding Theory Design Guide Handbook			1.30.021		
EMC Performance Requirements and Test Methods			1.30.022		
Digital Computer System Grounding			1.30.024		
Catergory - DOCUMENTATION					
Joint Glossary of Technical Terms	JNT-STD 10-03		1.01.006		
Graphic Symbols for Logic Diagrams	JNT-STD 32-01	2-04-02	1.41.104		
Hardware Product Configurator			1.01.004		
Equipment Configuration Identification and Control			1.01.007		
Equipment Documentation Requirements			1.01.008		
Terminology for Referencing American National Standards			1.10.010		
Graphic Symbols for Electrical and Electronic Diagrams	JNT-STD 32-02	2-04-01	1.41.101		

Title	JNT or Industry No.	NCR No.	CDC No.	Applicable Standard	Option Selected
Reference Designations for Electrical and Electronic Parts and Equipment			1.41.102		
Product Support Manuals			1.50.001		
Flowchart Symbols and Usage	X3.5-1970		1.80.003		
Microcircuit Handbook			15006100		
Software Development Document			1.01.103		
IMS			1.01.104		
ERS			1.01.105		
Software Identification			1.01.101		
Controlware Identification & Control			1.01.102		

12.4 APPENDIX D - CONFIGURATIONS

The configurations assumptions and component characteristics were used as the base to calculate the RAS objectives, Performance Objectives, and Cost Objectives.

General Remarks

- The system configurations shown are representative systems. Optimal configuration for each installation, as a function of its application environment, may deviate significantly from the typical system.
- Only single-mainframe system configurations are included at this time, multi-mainframe configurations will be added.
- New peripheral products, e.g., Mass Storage Subsystem, non-impact printer, helical scan tapes, swapping memory,etc. will be included as design specifications become firm.

12.4.1 SYSTEM CONFIGURATIONS

12.4.1.1 S0 System

S0 SYSTEM			
MAJOR COMPONENT	ENTRY	MEDIUM	LARGE
P1 Processor	1	1	1
M1 Memory	512KB	1MB	2MB
Data Module Disk Drive	2 Sp.	6 Sp.	10 Sp.
50ips Tape Drive	0	2	3
600cpm Card Reader	1	1	1
600lpm Line Printer	1	1	0
900lpm Line Printer	0	1	2
Communication Lines	2	4	6
SUPPORTING COMPONENT	ENTRY	MEDIUM	LARGE
SP Processor	1	1	1
Flexible Disk	1	1	1
Console W/CRT, Printer	1	1	1
Integrated Disk Controller	1	1	2
Tape Controller (50 ips)	0	1	1
Serial Channel Adapter	1	1	1
Network Interface	1	1	1

12.4.1.2 S1 System

S1 SYSTEM

MAJOR COMPONENT	ENTRY	MEDIUM	LARGE
IP1 Processor		2	4
IM1 Memory		1.5MB	4MB
Data Module Disk Drive		6 Sp.	12 Sp.
8-Byte Disk		1 Sp.	2 Sp.
200ips Tape Drive		3	4
600cpm Card Reader		1	1
600lpm Line Printer		2	1
2000lpm Line Printer		0	1
Communication Lines		10	20

SUPPORTING COMPONENT	ENTRY	MEDIUM	LARGE
ICA		2	12
SP Processor		2	2
Flexible Disk		2	2
Console W/CRT,Printer		1	2
Integrated Disk Controller		1	0
Disk Controller		1	4
Tape Controller (200 ips)		1	2
Serial Channel Adapter		1	3
Comm. Controller (20 lines)		1	1

* Overlaps the S0 range, not defined.

12.4.1.3 S2 System

S2 SYSTEM

MAJOR COMPONENT	ENTRY	MEDIUM	LARGE
IP2 Processor	1	1	2
IM2 Memory	2MB	4MB	6MB
Data Module Disk Drive	6 Sp.	12 Sp.	16 Sp.
8-Byte Disk Drive	1 Sp.	2 Sp.	4 Sp.
200ips Tape Drive	3	4	4
150 IPS Tape Drive	1	1	1
600cpm Card Reader	1	2	2
900lpm Line Printer	0	1	0
2000lpm Line Printer	1	1	2
Communication Lines	12	20	50

SUPPORTING COMPONENT	ENTRY	MEDIUM	LARGE
CMA	1	2	2
IIB	1	2	2
SP Processor	2	2	2
Flexible Disk	2	2	2
Console W/CRT, Printer	1	2	2
Disk Controller	2	4	6
Tape Controller (200 ips)	1	2	2
Tape Controller (50 ips)	1	1	1
Serial Channel Adapter	2	3	4
Comm. Controller (20 lines)	1	1	1
Comm. Controller (30 lines)	1	1	1
MG Set	1	1	1
Refrigeration Unit	1	1	2

12.4.1.4 S3 System

S3 SYSTEM			
MAJOR COMPONENT	ENTRY	MEDIUM	LARGE
P3 Processor	1	1	2
M3 Memory	4MB	6MB	10MB
Data Module Disk Drive	8 Sp.	10 Sp.	16 Sp.
8-Byte Disk Drive	2 Sp.	4 Sp.	6 Sp.
1200ips Tape Drive	4	6	6
1600cpm Card Reader	2	2	2
900lpm Line Printer	1	2	1
2000lpm Line Printer	1	1	2
Communication Lines	20	50	100
SUPPORTING COMPONENT	ENTRY	MEDIUM	LARGE
CMA	2	2	2
ITB	2	2	2
SP Processor	2	2	2
Flexible Disk	2	2	2
Console W/CRT, Printer	2	2	2
Disk Controller	4	4	6
Tape Controller (200 ips)	2	2	2
Serial Channel Adapter	3	4	5
Comm. Controller (20 lines)	2	1	0
Comm. Controller (40 lines)	0	1	3
MG Set	1	1	2
Refrigeration Unit	1	1	2

12.4.1.5 S4 System

S4 SYSTEM			
MAJOR COMPONENT	ENTRY	MEDIUM	LARGE
P4 Processor	1	1	2
M3 Memory	8MB	12MB	16MB
Data Module Disk Drive	12SP	16 Sp.	24 Sp.
8-Byte Disk Drive	4SP	6 Sp.	8 Sp.
1200ips Tape Drive	6	6	8
1600cpm Card Reader	2	2	2
2000lpm Line Printer	3	3	4
Communication Lines	50	100	150
SUPPORTING COMPONENT	ENTRY	MEDIUM	LARGE
CMA	2	2	4
ITB	2	2	4
SP Processor	2	2	4
Flexible Disk	2	2	4
Console W/CRT, Printer	2	2	2
Disk Controller	4	6	8
Tape Controller (200 ips)	2	2	2
Serial Channel Adapter	4	6	8
Comm. Controllers (40 lines)	2	3	4
MG Set	2	2	2
Refrigeration Unit	2	2	3

12.4.2 COMPONENT CHARACTERISTICS

12.4.2.1 CPU's

Processor	MLB	Inherent MTBF (Hrs)
P1 Central Processor (with options)	$ 24,327 (3)	1,608
P2 Central Processor (no options)	70,163 (1)	1,377
P3 Central Processor (no options)	152,078 (1)	2,500
P4 Central Processor (no options)	293,656 (2)	1,000

Notes:
(1) CDC 1980/90% Slope/35th Unit/6% Inflation Factor
(2) CDC 1976/90% Slope/10th Unit/6% Inflation Factor
(3) NCR 92% Slope/Cum Ave. Cost (3000 Unit Total/Midpoint 1979, P1 MLB including one ITB subsystem.

Memory	MLB (3)	Inherent MTBF (4)
M1-512K	$ 9,010	4,457
M1-1M		
M1-1.5M		
M1-2M		
M1-4M	73,000	
M2-2M (2)	87,000	3,514
M2-4M (2)	126,000	2,391
M3-4M (2)	170,000	2,214
M3-6M (2)	213,000	1,714
M3-8M (2)	246,000	1,502
M4-8M (2)	302,000	1,361
M4-12M (2)		1,041
M4-16M (2)	412,000	917

Notes:

(1) The above costs assume 6% annual inflation from 1974 to 1980 and 90% slope/35th unit.

(2) Assume one 32 bit port and one 64 bit port.

(3) Cost assumptions on 4K RAM, substantial cost reduction expected for 16K RAM.

(4) Assumes a chip failure rate of .5 failures/million hours.

12.4.2.2 Peripheral Equipment

Disk Drives	1978 FLC(1)	Inherent MTBF
9770 Data Module Drive (420MB)	$10,631	500
Billion-Byte Drive		**

** = No current data available

Magnetic Tape Drives	1978 FLC(1)	Inherent MTBF
200 ips, GCR	9,850	500
50 ips	2,960	500

None of these drives include a controller.

Printers	1978 FLC(1)	Inherent MTBF
Fastrain 2000 lpm	24,169	600
Band Printer 600lpm	5,100	600
Band Printer 900 lpm	6,200	600

The above printers include controller cost.

Card Equipment	1978 FLC(1)	Inherent MTBF
LCR 500/600/800 cpm reader	$ 1,445	1,000

12.0 APPENDICES
12.4.2.2 Peripheral Equipment

The ECR reader includes interface and controller.

12.0 APPENDICES
12.4.2.2 Peripheral Equipment

Controllers	1978 FLC(1)	Inherent MTBF
Tape Controller (50 ips)	$ 4,000	2,850
Tape Controller (200 ips)	12,000	2,850
Integrated Controller for 9770 Data Module Drives	5,000	16,031*
Low Cost Network Interface (10 lines total)	5,000	9,755*
Freestanding Communications Controller		
- 20 lines	10,000	2,000*
- 30 lines	12,000	2,000*
- 40 lines	14,000	2,000*

* = Does not include communication lines.

Notes:

1) Fully loaded cost exclusive of amortization of start-up cost.

12.4.2.3 I/O and Maintenance Subsystem

Subsystem	MLB	Inherent MTBF
ITB	$ 8,932	2,451
ICA (Pair)	1,700	33,333
CMA	2,400	29,185
SP Processor	2,006	36,429
Console W/CRT, Printer	2,733	3,685 **
Flexible Disk	418	78,100

** - MTBF does not include thermal printer

Channels and Adapters	MLB	Inherent MTBF (Hrs)
Serial Channel Adapter (including Channel Controller)	2,360	56,405

12.4.2.4 Communication Lines and Terminal Equipment

12.4.2.5 External Equipment

External Equipment	MLB	Inherent MTBF (Hrs)
MG Set	$ 9,000	
Refrig. Unit	$ 6,000	

12.5 APPENDIX E - COST PERFORMANCE GRAPHS

The cost/performance objectives for IPL are those defined in section 7 of the NCR/COC Requirements and Goals document. The data presented in this appendix is a direct excerpt from that document and is intended to be fully compliant.

GENERAL

This section specifies cost/performance requirements for each IPL system model, established in terms of the total product line range. These requirements consider each model on a system basis (i.e., performance is specified on a system thruput basis, and costs specify the total manufacturing cost of central system hardware) with the intent of establishing an aggregate baseline objective for each model, against which design tradeoffs can be made. Consequently, no allocations of these requirements to individual hardware and software subsystems are specified or implied in either this section or other portions of this document. Such allocations are the responsibility of ASL and the implementing divisions and are beyond the purview of Requirements and Goals.

IPL cost/performance requirements are specified in the form of a set of curves on cost versus performance charts ("Workload Performance Charts") (Section 7.3). This format is identical to CDC's statement of requirements (Memo to D. L. Slais from G. M. Beaugonin, no subject, January 17, 1974) and is used for three basic reasons:

1. Ease of relating to other systems in assessing relative cost/performance.
2. Graphic portrayal of the intent to cover the IPL range continuously; e.g., without cost/performance gaps.

GENERAL

3. Reflection of the fact (by use of logarithmic scales) that requirements are more sensitive for the smaller models than for the larger models.

In addition to the requirements per se, a formal definition of the charts (section 7.2) is included to facilitate interpretation. From this definition several points must be emphasized:

1. The curves do not specify cost/performance lines on which "average" or "target" configurations must lie. Instead, they bound the acceptable cost/performance region for system configurations capable of achieving the specified performance. Such configurations need only incorporate the minimum central memory, unit record equipment and disk storage drives necessary to be fully functional (including deadstart and diagnostics) and to achieve that performance level. Consequently, under this groundrule, data base storage capacity and configuration capability may be inadequate for the user environment. Further, magnetic tape is not a configuration requirement herein; e.g., all workloads must be structured for use of rotating mass storage.
2. Workloads are assumed to include a combination of both compilation and execution.
3. IPL peripherals as defined in Section 5.3 (Appendix B), are the only devices assumed, to include an anticipated 210MB Data Module. Therefore,

GENERAL

3. (Cont'd)
no consideration is made with respect to advances in secondary storage technology. The availability of such devices may have considerable cost impact, but will not affect the performance ranges of the various IPL system models because it is assumed that a sufficient number of mass storage devices are provided to achieve desired CP utilization.

4. Five system models are specified. The IPL range can be completely covered utilizing four equally-spaced processors, P1-P4, and the corresponding system models, S1-S4. Configurations for system model Sn incorporate one or more Pn processors plus at least one P1 processor, to include S1 configurations requiring a minimum of two P1 processors.
The fifth system model, S0, is included to provide a distinct, low cost, uniprocessing entry offering. S0 configurations employ only one P1 processor.

5. These curves are established for a 1979 datum. Costs applicable to products introduced in other years are adjusted to 1979 on a learning curve basis only; i.e., the impacts of technology shifts and inflation are not considered.

6. These cost performance goals are based on the final report (dated January 1975) of a cost/performance requirements study conducted by an NCR/CDC team.

REQUIREMENTS FORMAT

The cost/performance requirements in Section 7.3 are specified as a set of Workload Performance Charts, each of which is associated with one of the following operating environments:

1. Commercial Multiprogramming Batch
2. Scientific Multiprogramming Batch
3. Transaction Processing
4. Interactive Time-Sharing

The form of these charts is shown in Figure 7.2-1. Each chart contains a curve, plotting performance against cost. The curve spans that portion of the IPL range for which cost/performance requirements are established for the corresponding operating environment.

Each curve divides the cost/performance domain into acceptable and unacceptable regions; e.g., the curve does not specify a line on which IPL models must lie. Further, for a configuration to lie in the acceptable regions, it must only be capable of achieving the desired performance level and need not necessarily contain adequate data base storage. In other words, the curve does not imply "target" or "average" configurations.

Each curve is divided into a maximum of five subranges, each of which defines the range for the corresponding IPL system model (S0-S4). Each subrange is the theoretical maximum, identified by the intersection

REQUIREMENTS FORMAT {Cont'd}

of the curve with a pair of asymptotic lines. The latter are defined in terms of the corresponding Central Processor models {e.g., Pn corresponds to Sn, except that P1 also corresponds to S0}:

1. Sn Minimum System Cost Asymptote {"Sn Min"}. This line specifies the minimum cost configuration utilizing one Pn Central Processor, which can be expected to function in the respective operating environment.
2. Sn Maximum Performance Asymptote {"mPn Max"}. This line establishes the maximum theoretical performance any configuration utilizing the Pn Central Processor can achieve in the respective operating environment {e.g., 100% Central Processor utilization on user tasks}. For uniprocessing curves, the configuration contains one Pn {e.g., n=1, except for S1, where m=2}; for multiprocessing curves, four Pn's {e.g., m=4}.

There is no requirement for the Sn system model to be underneath the cost/performance curve to the extremes of its subrange. However, it must overlap with the adjacent models, Sn-1 and Sn+1, beneath the curve.

Each curve applies to all workloads characteristic of the operating environment to which the chart applies. Section 7.4 elaborates on this requirement.

All curves are established for a 1979 datum.

REQUIREMENTS FORMAT

To facilitate comparison with CDC scientific environment goals expressed in terms of processor-memory costs only, the following additional data is provided.

The cost/performance chart for scientific environment {figure 7.3-2} contains an additional curve not found on the other charts. The additional curve plots performance against processor and memory costs only; that is, the cost of peripherals has been removed from the standard curve, producing a second curve translated downward on the graph from the standard curve.

Also, the goal for best cost/performance {ratio is minimum at the point described} for each of the systems, S0 through S4, for scientific environment is as follows:

System	Relative Performance *	System Cost **	Processor-Memory Cost **
S0	.85	$67.6K	$ 43,073
S1	1.3	82.7K	56,188
S2	3.8	207K	142,660
S3	9.7	341K	276,669
S4	26.9	566K	496,268

* Relative to a CDC 6400 {CYBER 73}.

** As stated in section 7.1, costs are based on January 1975 data. Currently observed memory costs are less than shown for 4K chips. When 16K chips are introduced, another 50% decrease over currently observed costs can be expected.

REQUIREMENTS FORMAT

FORM OF WORKLOAD PERFORMANCE CHART

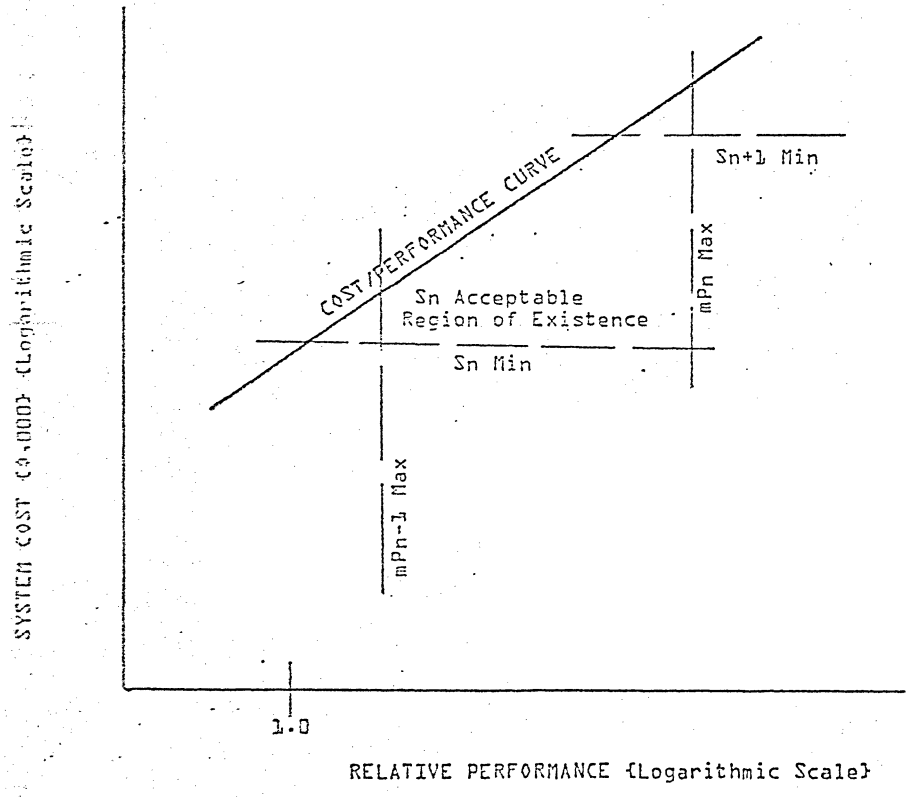


Figure 7.2-1

WORKLOAD PERFORMANCE CHARTS

This section contains charts showing the required cost/performance for IPL systems operating in each of the following environments.

1. Commercial Multiprogramming Batch
2. Scientific Multiprogramming Batch
3. Transaction Processing
4. Interactive Time-Sharing

The charts are explained in File 7.2.

In addition to the 1979 cost/performance curve, three additional curves have been plotted as indicated for years 1980, 1981 and 1982. These additional curves assume a 15% per year cost/performance enhancement from the 1979 curve. These plots represent cost/performance criteria for system models introduced in the corresponding year. The low end is not plotted past year 1980 since it is expected to be introduced by 1980. Since these curves are a measure of system cost/performance at initial introduction of the system, it is not correct to apply a later year plot to a system introduced in a prior year.

WORKLOAD PERFORMANCE CHARTS

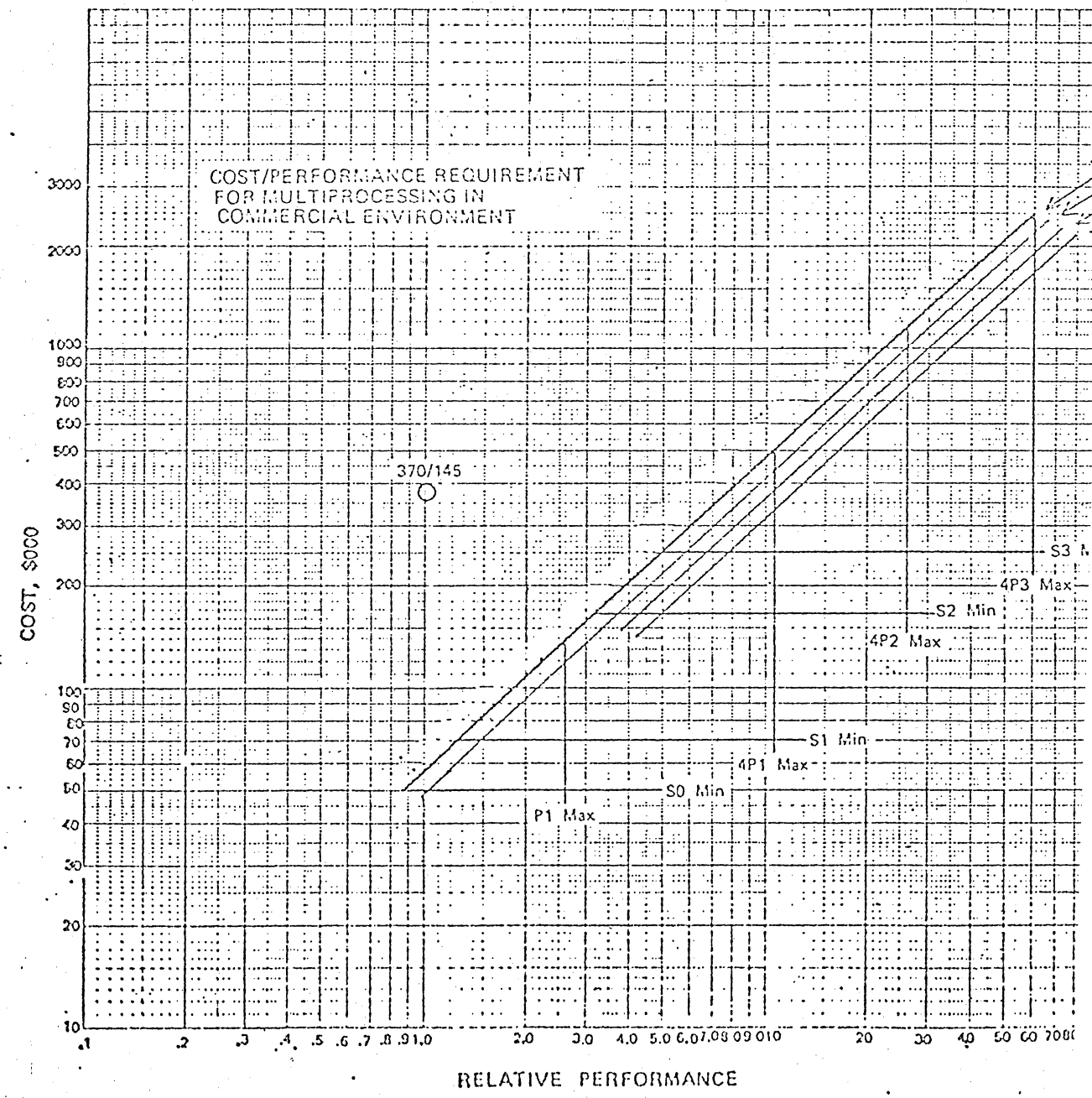


Figure 7.3-1 - Commercial Environment

WORKLOAD PERFORMANCE CHARTS

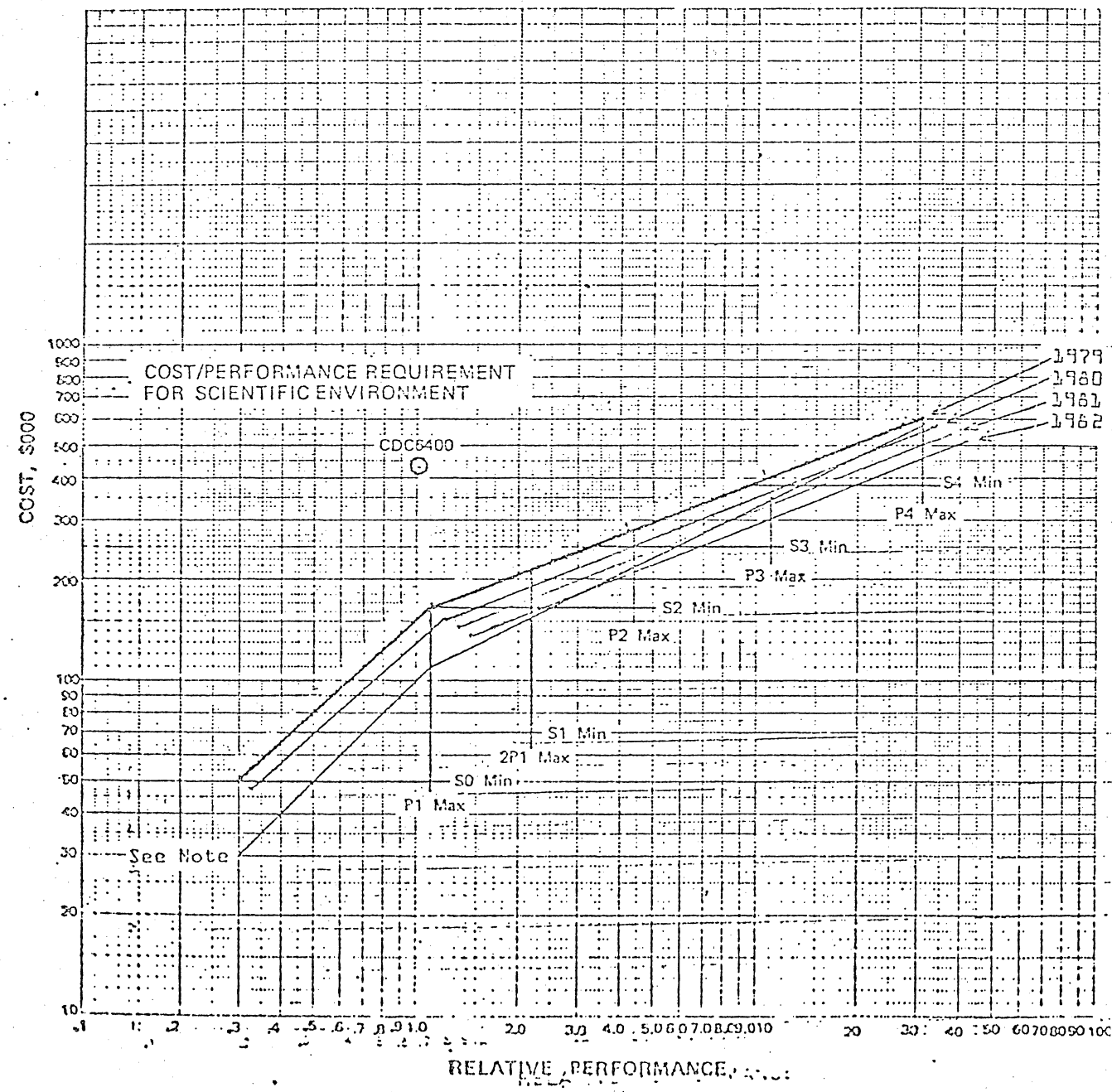


Figure 7.3-2 - Scientific Environment

Note: The bottom curve shows cost of pro
and memory only (see file 7.2).

WORKLOAD PERFORMANCE CHARTS

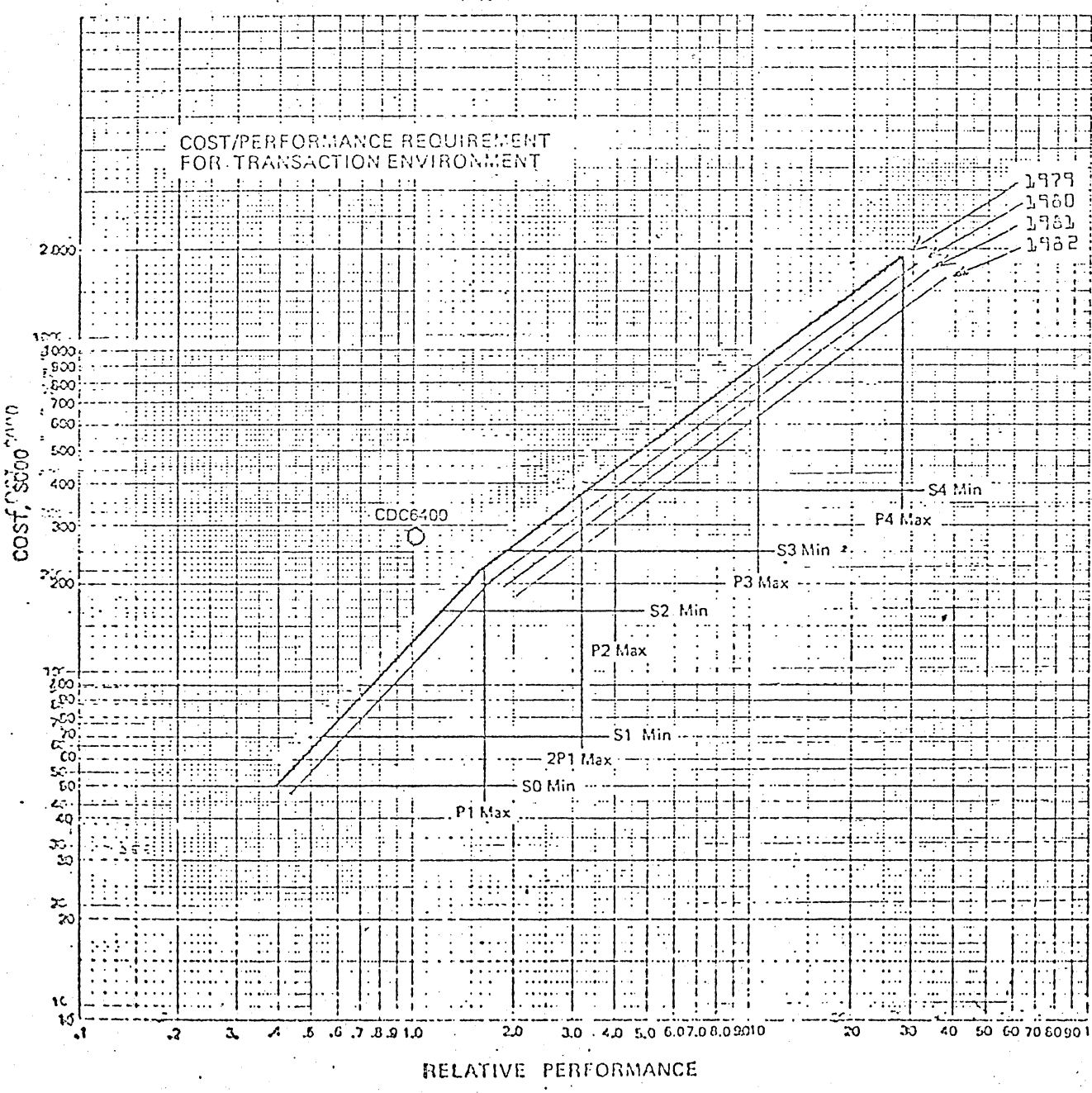


Figure 7.3-3 - Transaction Environment

WORKLOAD PERFORMANCE CHARTS

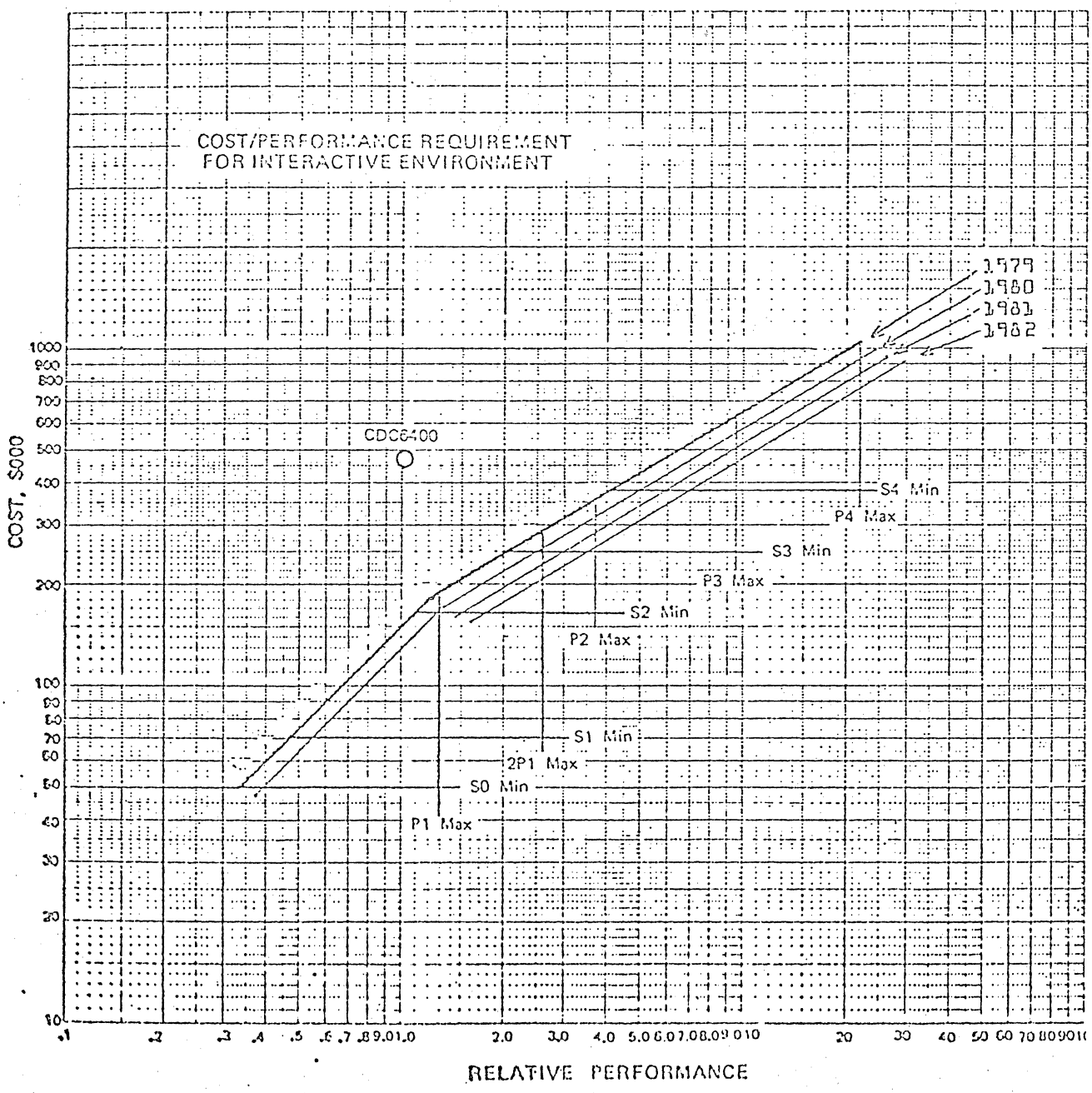
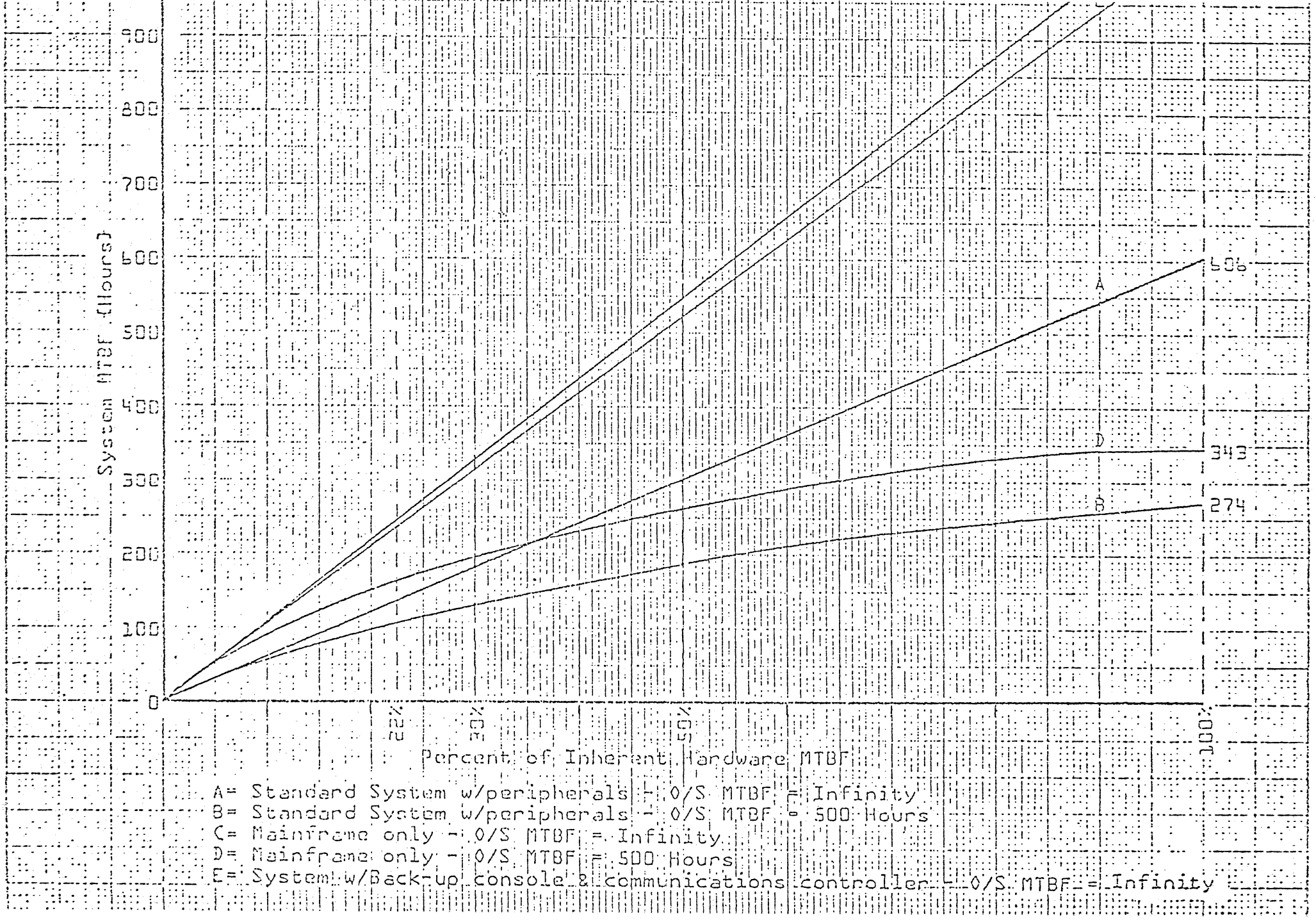
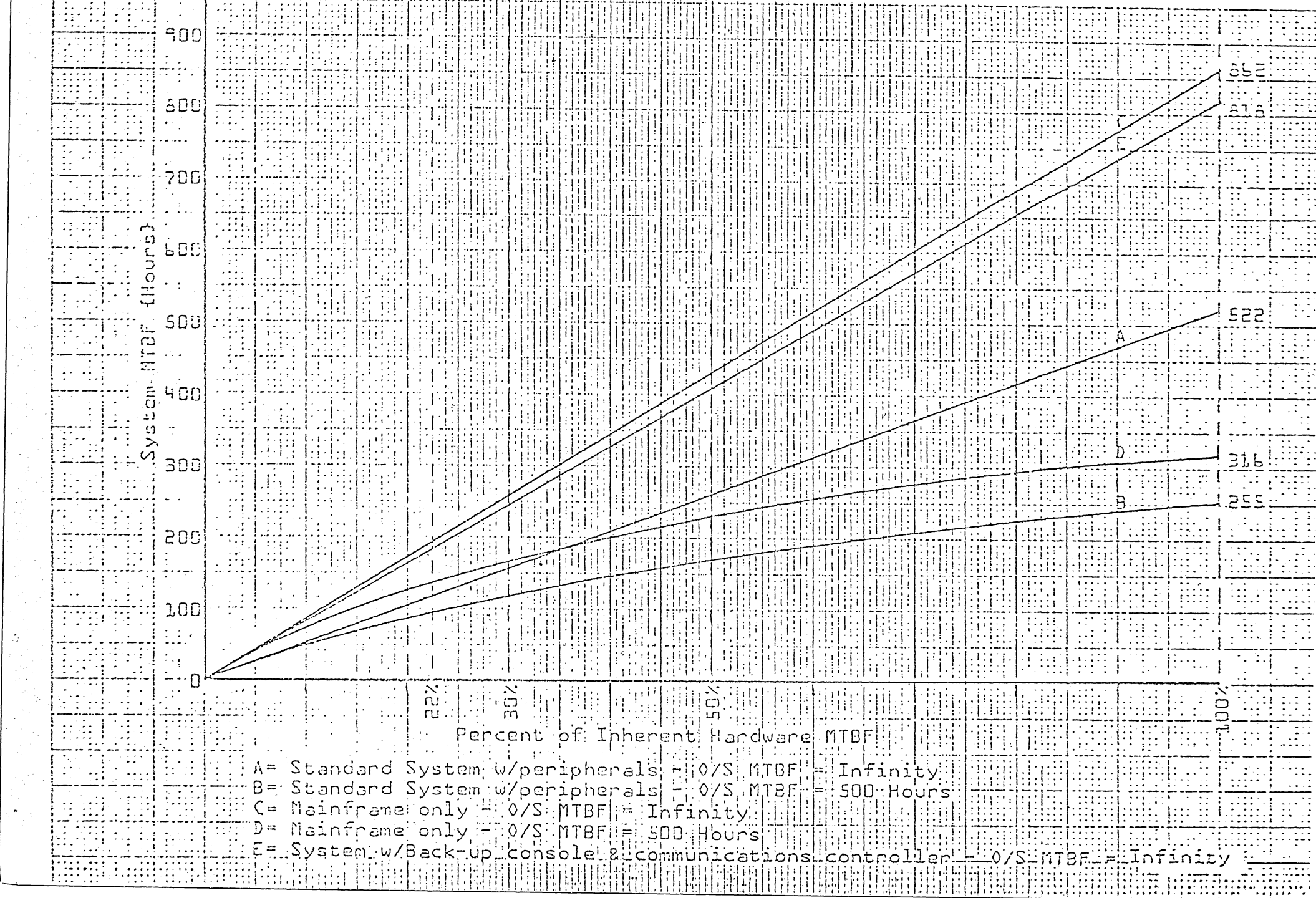


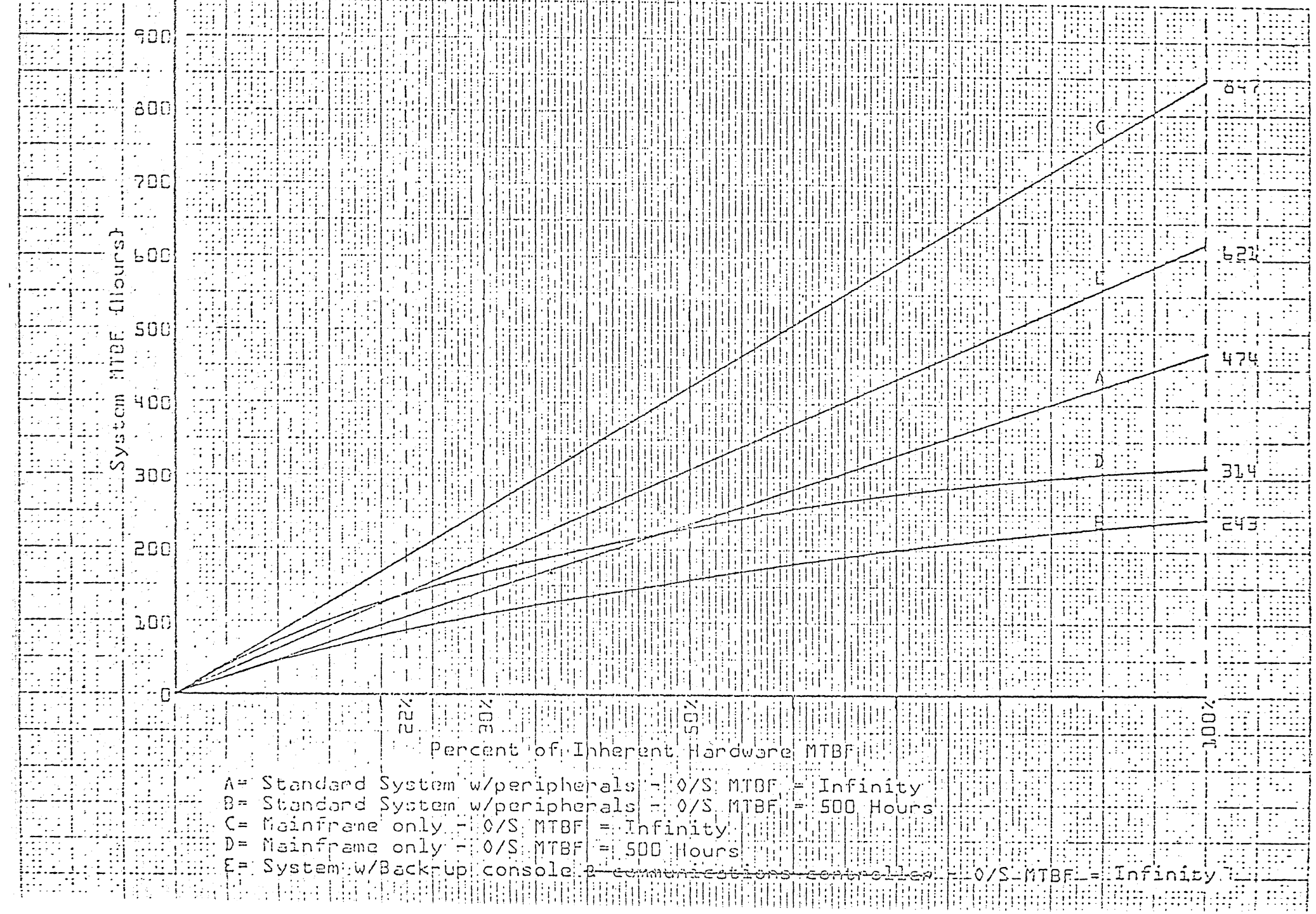
Figure 7.3-4 - Interactive Environment

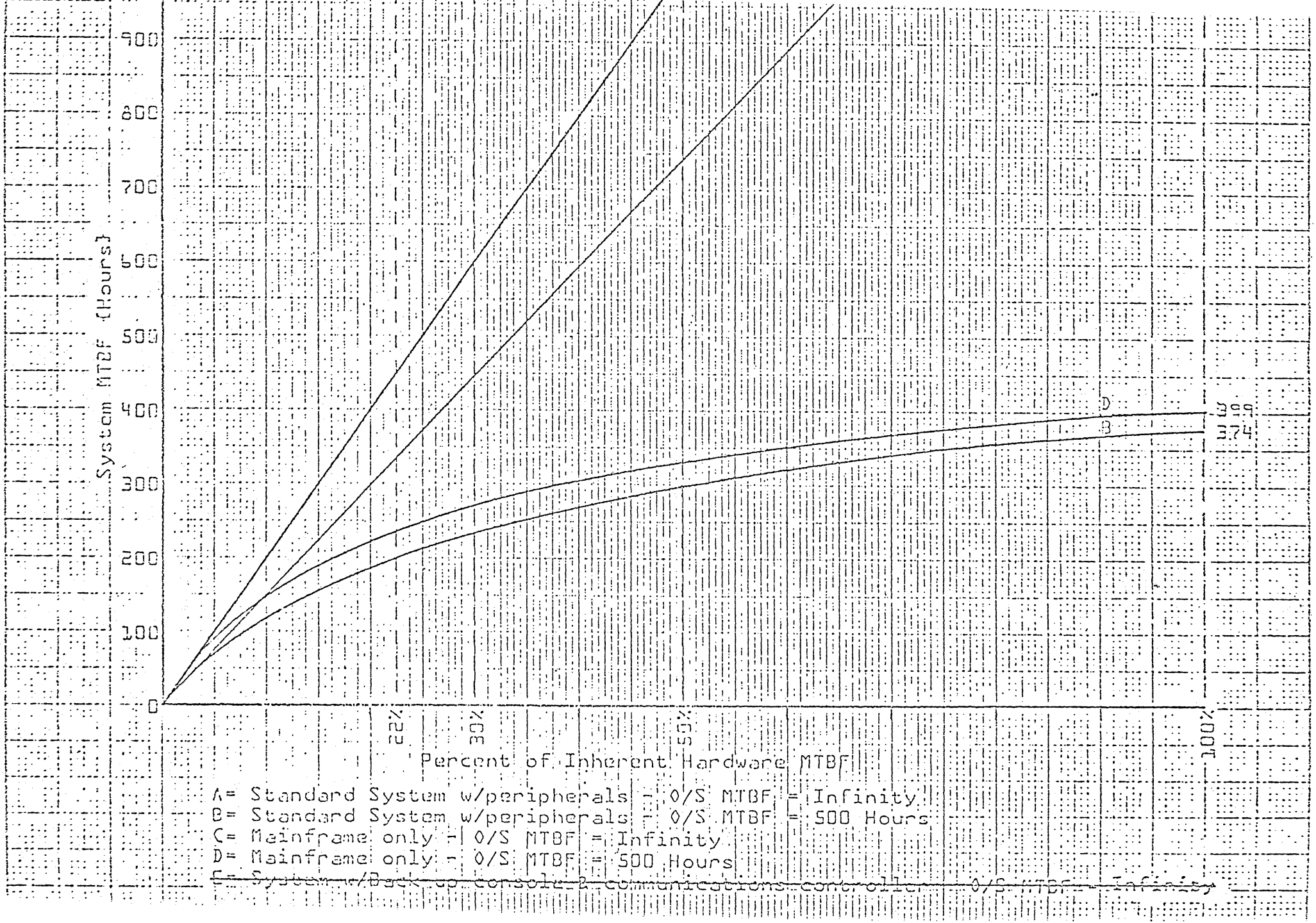
12.6 APPENDIX F - SYSTEM MTBF CURVES

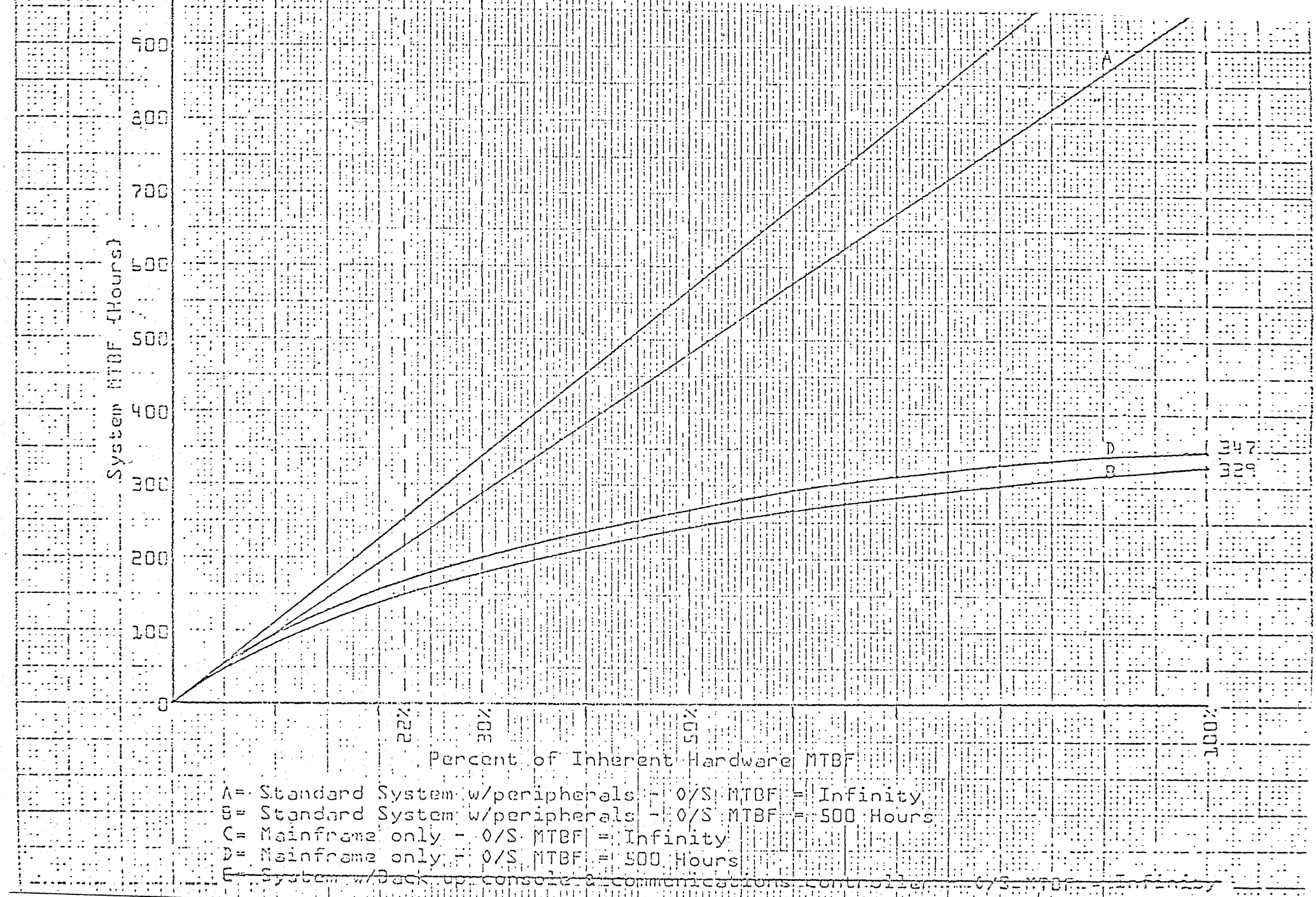
The graphs presented in this appendix give detailed information about system hardware MTBF projections. The curves have been calculated for the "Medium" system configurations of Appendix D using projected inherent MTBF's for those components.


System MTBF (Hours)
900
800
700
600
500
400
300
200
100
0
A
D
B
506
343
274
22%
33%
50%
100%
Percent of Inherent Hardware MTBF
A= Standard System w/peripherals - O/S MTBF = Infinity
B= Standard System w/peripherals - O/S MTBF = 500 Hours
C= Mainframe only - O/S MTBF = Infinity
D= Mainframe only - O/S MTBF = 500 Hours
E= System w/Back-up console & communications controller - O/S MTBF = Infinity


System MTBF (Hours)
900
800
700
600
500
400
300
200
100
0
852
818
522
316
255
E
A
D
B
22%
30%
50%
100%
Percent of Inherent Hardware MTBF
A= Standard System w/peripherals - O/S MTBF = Infinity
B= Standard System w/peripherals - O/S MTBF = 500 Hours
C= Mainframe only - O/S MTBF = Infinity
D= Mainframe only - O/S MTBF = 500 Hours
E= System w/Back-up console & communications controller - O/S MTBF = Infinity


900
800
700
600
500
400
300
200
100
0
System MTBF (Hours)
847
621
474
314
243
C
E
A
D
B
22%
30%
50%
100%
Percent of Inherent Hardware MTBF
A= Standard System w/peripherals - O/S MTBF = Infinity
B= Standard System w/peripherals - O/S MTBF = 500 Hours
C= Mainframe only - O/S MTBF = Infinity
D= Mainframe only - O/S MTBF = 500 Hours
E= System w/Backup console & communications controller - O/S MTBF = Infinity


System MTBF (Hours)
900
800
700
600
500
400
300
200
100
0
22%
30%
50%
100%
Percent of Inherent Hardware MTBF
D
B
399
374
A= Standard System w/peripherals - O/S MTBF = Infinity
B= Standard System w/peripherals - O/S MTBF = 500 Hours
C= Mainframe only - O/S MTBF = Infinity
D= Mainframe only - O/S MTBF = 500 Hours
E= System w/Back-up Console & Communications Controller - O/S MTBF = Infinity


System MTBF (Hours)
900
800
700
600
500
400
300
200
100
0
A
D
B
347
329
22%
30%
50%
100%
Percent of Inherent Hardware MTBF
A= Standard System w/peripherals - O/S MTBF = Infinity
B= Standard System w/peripherals - O/S MTBF = 500 Hours
C= Mainframe only - O/S MTBF = Infinity
D= Mainframe only - O/S MTBF = 500 Hours
E= System w/Back up Console & Communications Controller - O/S MTBF = Infinity